



A Spatial Computing Architecture for Implementing Computation Circuits

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Overview

- Introduction
- Architecture
- Tools
- Preliminary Results
- Conclusions



Introduction

- **Computational Circuits**
 - Software converted to hardware for performance
 - ex. molecular dynamics, rendering, encoding, ...
 - Word-oriented circuits
- **Circuits can be very large**
 - Synthesis and Simulation have long runtimes
 - Wastes designer productivity
- **Research Objective**
 - Quickly compile and run computational circuits
 - Build a spatial computer



Introduction

- **Computational Circuits on FPGAs**
 - FPGAs bring simulation speed to $\frac{1}{4}$ ASIC
 - Problem 1: **Long Synthesis Time**
 - Synthesis down to gate level
 - Hinders incremental debugging and development
 - Problem 2: **Hard Capacity Limit**
 - Software accustomed to “infinite resources” model
 - Run a few more instructions
 - Add a few MB of memory
 - Add a few million gates ???



Introduction

- Architecture and Tools to implement computational circuits
 - Custom Architecture
 - Fast Tools
- Architecture+Tools address **synthesis time** and **capacity** problems



Introduction

- **Goals**
 - 10x faster than FPGA CAD tools
 - Minutes, not hours, for large design
 - Compile+Place+Route runtime like a software compiler
 - 10x capacity of an FPGA
 - Gracefully increase capacity at expense of speed
 - No less than 1/10th the speed of FPGA
 - Slower only at “full capacity”
 - As fast as FPGA at “low capacity”

Architecture

- Architecture Summary

- 2D Array of Processing Elements (PEs)

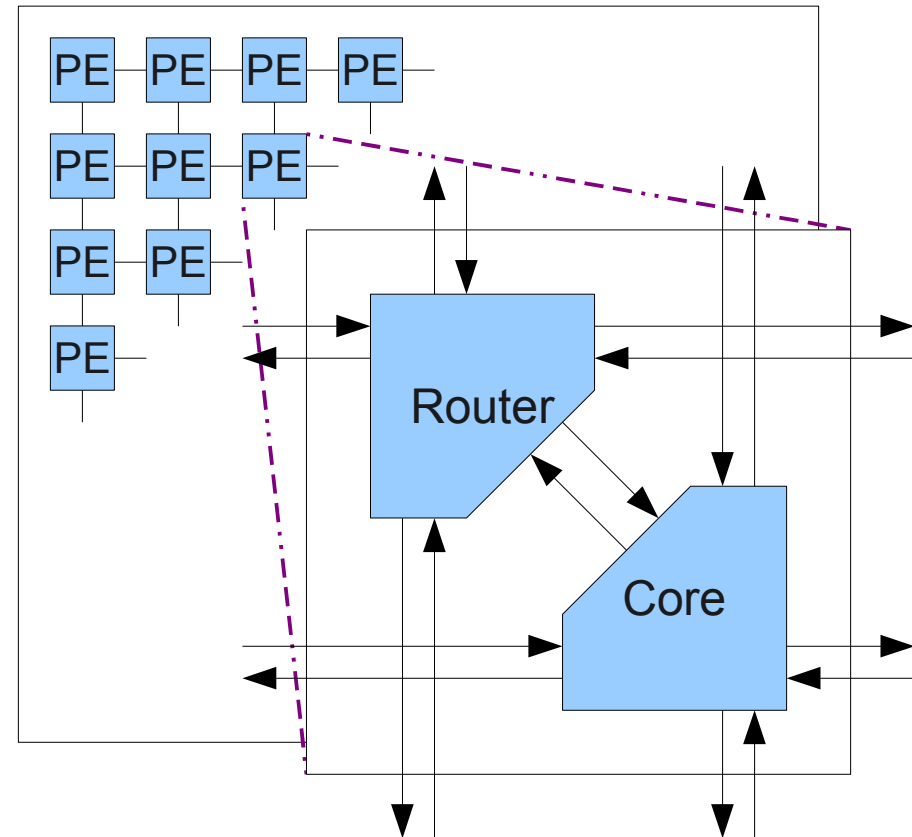
- PE is a small, fast sequential computer
- 3 GHz

- Mesochronous clock network

- Known phase mismatch between neighbours is negligible

- n cycle fixed schedule

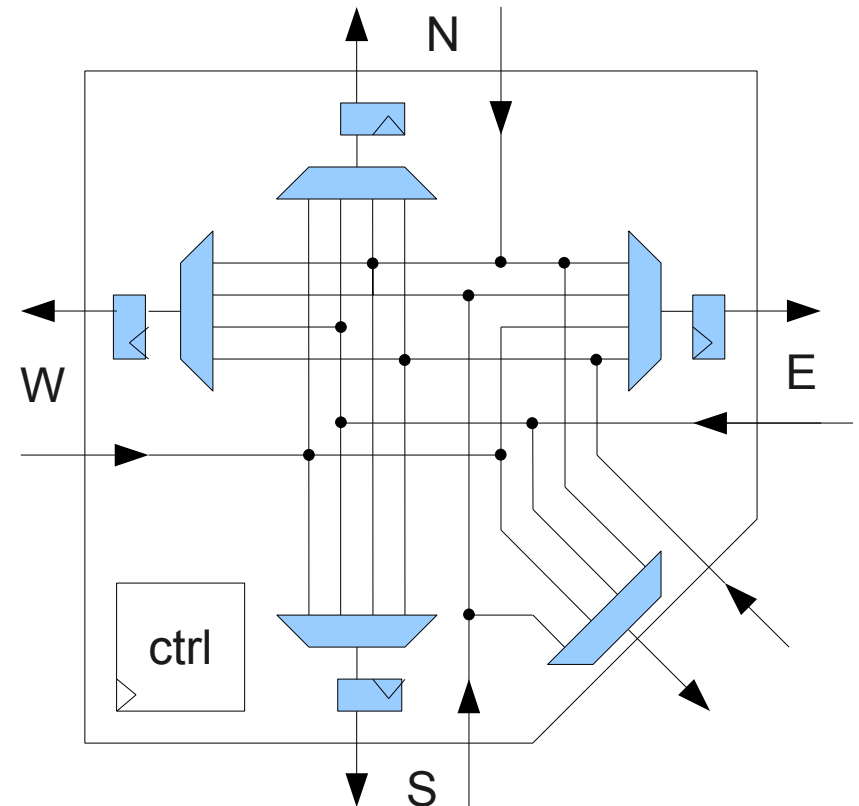
- One user cycle



- PE Router

- 5 x 5 data crossbar
- Fixed static schedule
- Pipelined interconnect
- PE accepts 1 write/cycle

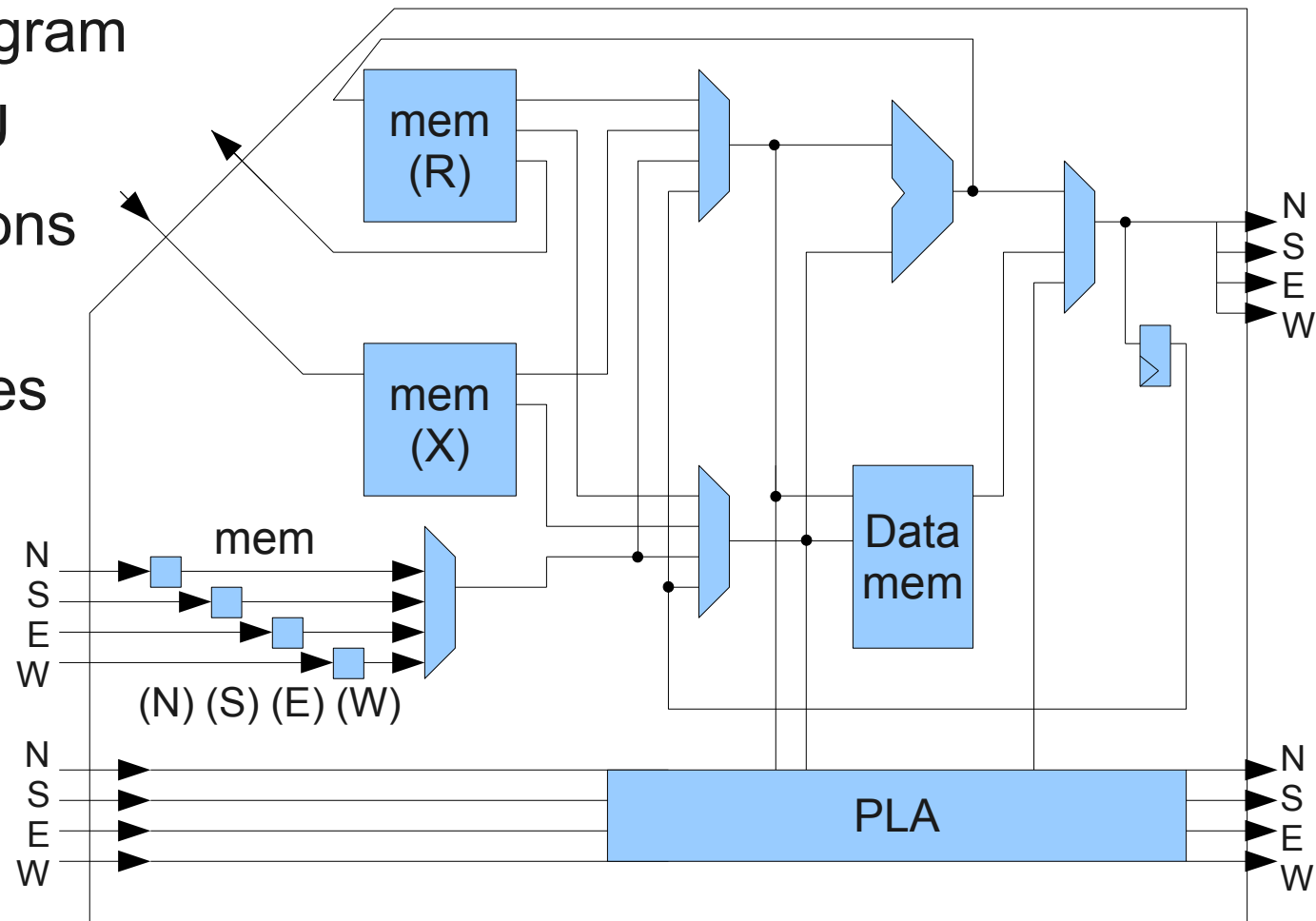
N	S	E	W	PE	Raddr	Waddr
S	PE		PE		4	
		W		N		6
...



Architecture

- PE Core

- Fixed static program
- 1 time-mux ALU
- Direct connections to neighbours
- 6 node memories
- Data memory
- PLA for bitops





Architecture

- Architecture questions

- PE core

- Node memory sizes?
 - Memory size?
 - Heterogeneous (e.g., some columns have more memory)?
 - ALU width? 2-way static superscalar?
 - PLA size? Use LUTs instead?

- PE router

- Bus widths?
 - Number of routers per PE?



Tools

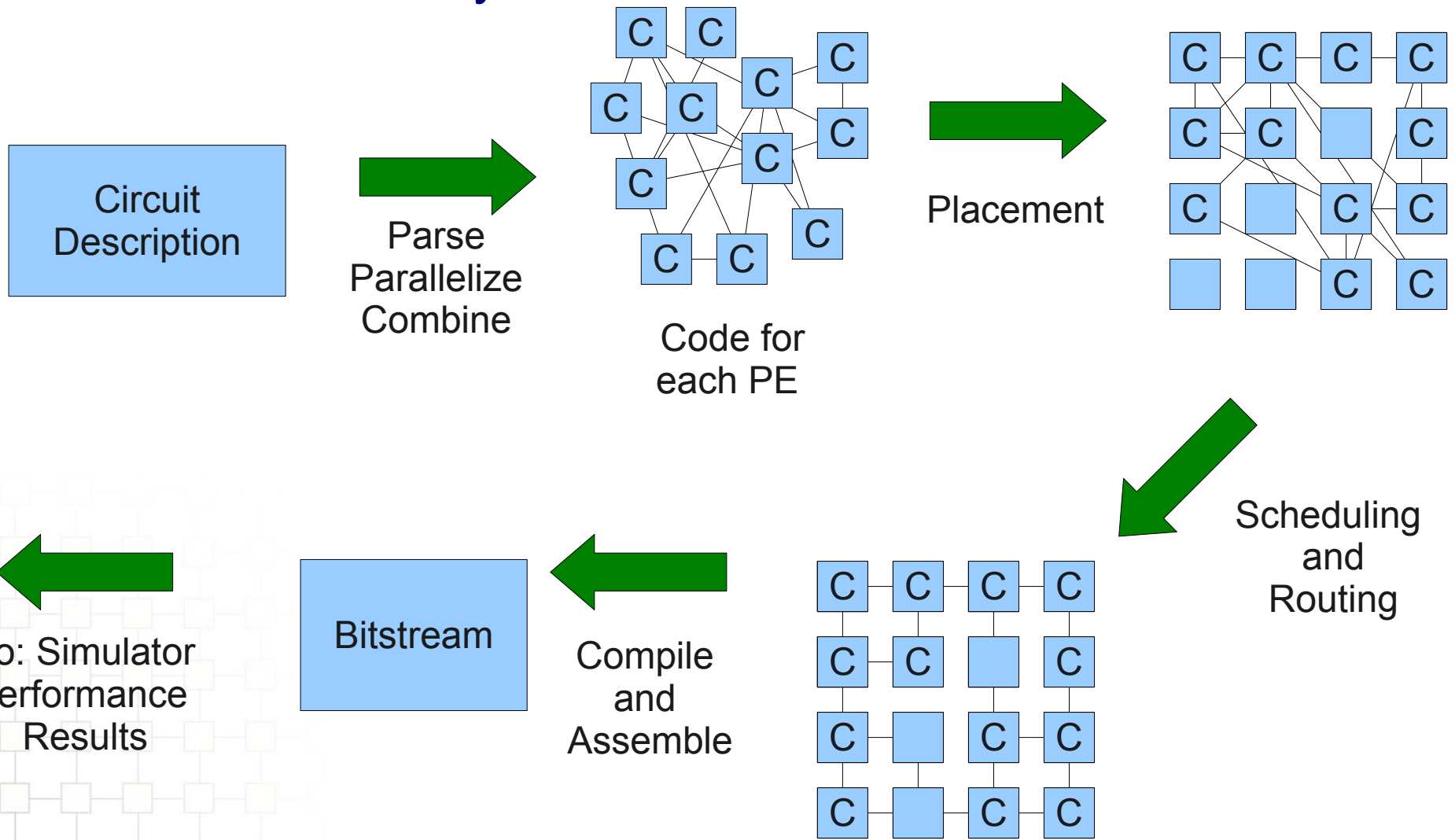
- **Fast tools**

- Behavioural compilation and word level synthesis
- ~1000 PEs to place and route in this architecture
- ~100,000 CLBs to place and route in FPGA

- **Tool flow**

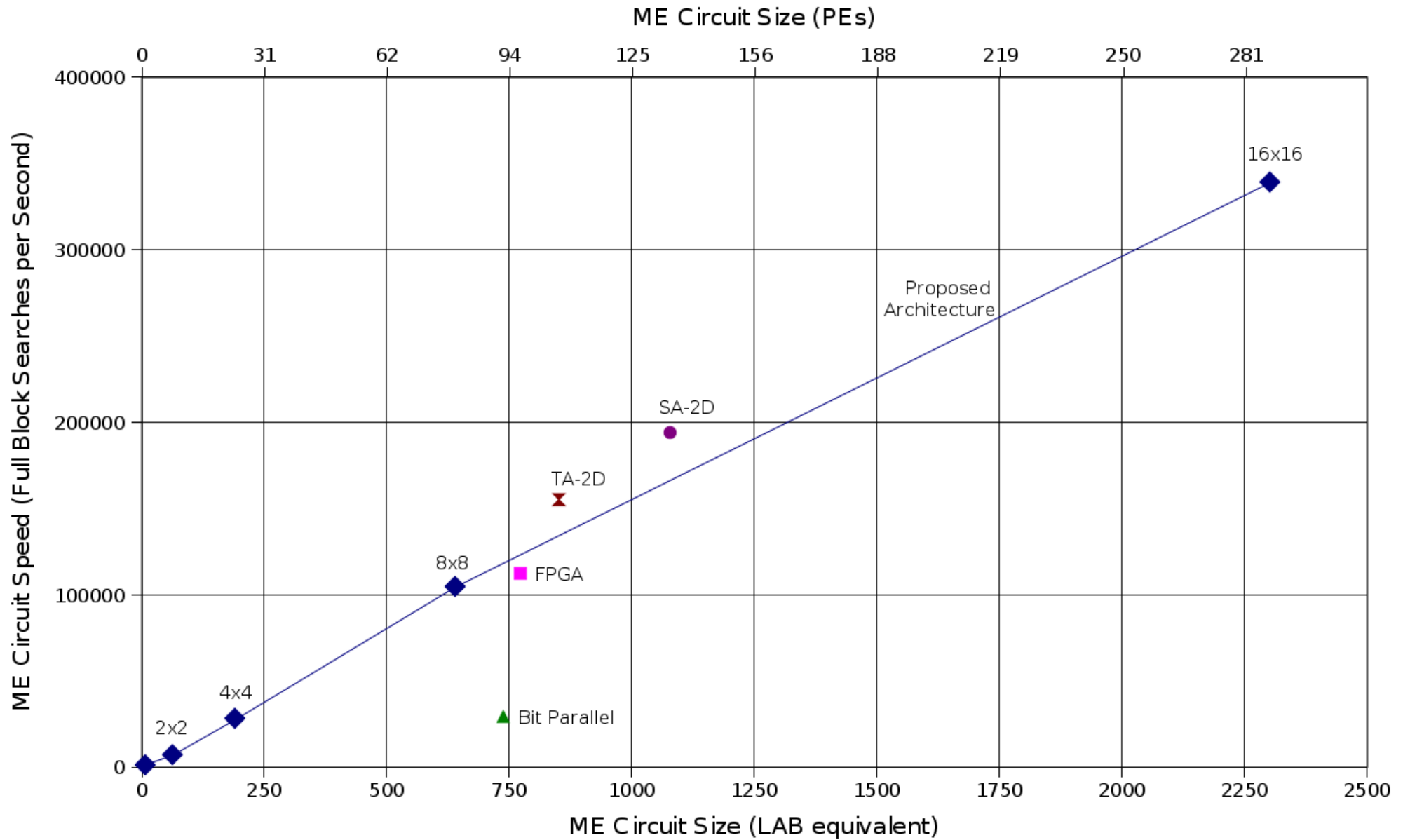
- Parallelize
- Combine
- Placement
- Schedule and Route
- Code Generation

- Tool Flow Summary





Preliminary Results





Thanks

- **Main Idea**
 - Take a computational circuit and compile+run it fast on a spatial architecture
- **Custom Architecture**
 - Time-multiplexed array-of-processors
 - High bandwidth, low latency communication
- **Fast Tools (Future Work)**
 - Behavioural compilation
 - Coarse grained architecture
- **Preliminary Results**
 - Shows performance vs. capacity tradeoff
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