Area, Delay, Power, and Cost Trends for Structured ASICs

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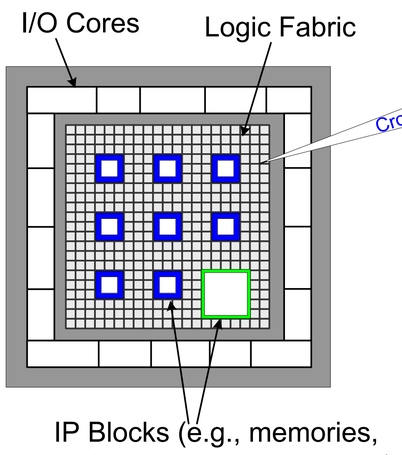
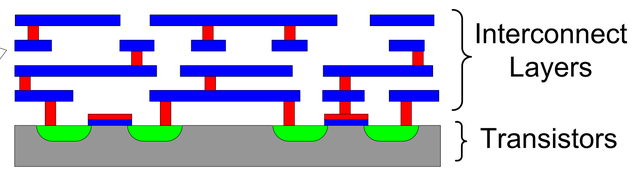
1. Motivation

- Current IC Design Issues
  - Enormous Design Effort
  - Huge NRE Costs
- Many ICs Still Manufactured with Old Processes
- FPGAs Not Always Suitable
  - Low Power, Hand-held Devices
  - Platform-based Designs, Analog or Hard IP
- Structured ASICs Promising, Little Research
  - Research Tools Needed, e.g. VPR for SAs

2. Structured ASICs

- ASIC-like Efficiency with FPGA-like Configurability
  - Metal + Via Programmable (MPSA), FPT2009 (this work)
  - Via-only Programmable (VPSA), FPGA2010 (coming soon)

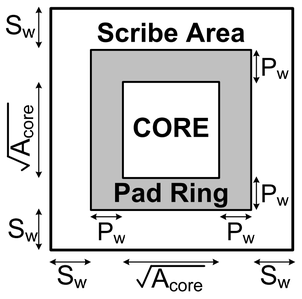




- **Standard-cell ASIC aka Cell-based IC**
  - All mask layers are customized for a design
- **FPGA**
  - All mask layers are prefabricated, shared by all designs
  - User design obtained by programming memory cells
- **Structured ASIC**
  - Most layers are prefabricated, shared by all designs
  - A few mask layers are customized for a design
  - User design fine-tuned by programming memory cells (optional)

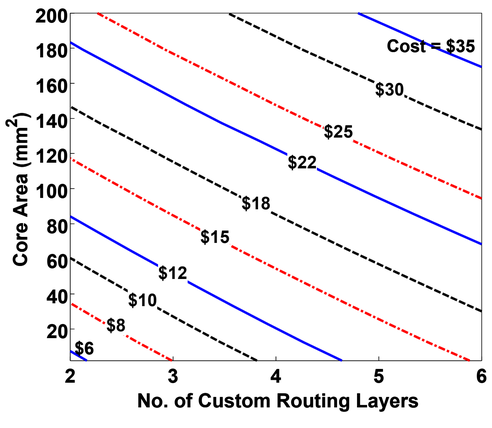
3. MPSA Die Cost

- Key Variables
  - Die Area and Yield: N_{gdpw} (good dies per wafer)
  - Custom Routing Layers: N_{rl}
- Key Fixed Parameters
  - Manufacturing Volume: V_{total}, V_{design}
  - Wafer Processing Costs: C_{wpm} *($ per mask)*
  - Mask Costs: C_{lower}, C_{upper} *($ per mask)*
  - Mask Layers: N_{lower}, N_{upper}



$$Cost_{die} = \frac{K_0}{N_{gdpw}} + N_{rl}\left(\frac{K_1}{N_{gdpw}} + K_2\right) + K_3$$

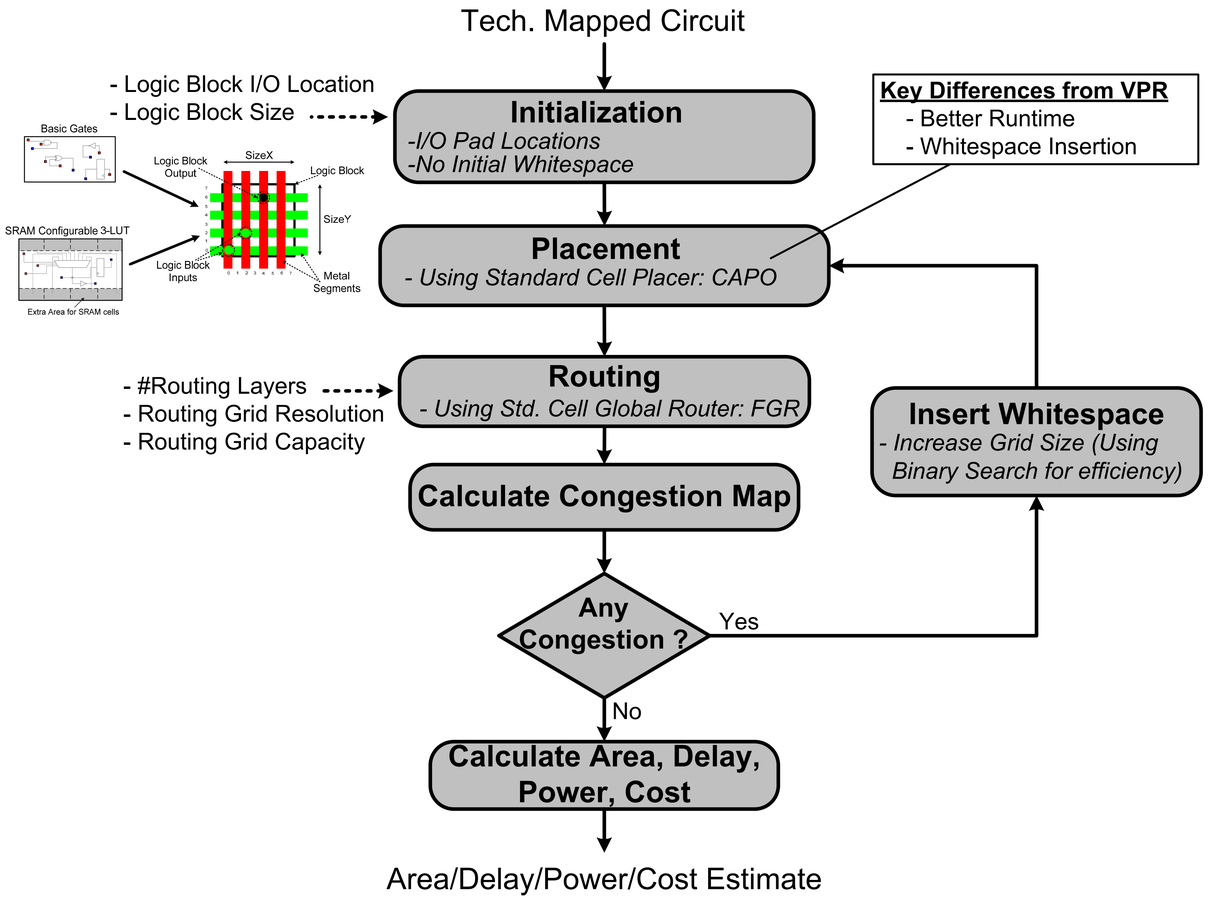
$C_{wpm}(N_{lower}+N_{upper})$ ~ $ 4000 ; $N_{mprl}C_{wpm}$ ~ $440 ; $\frac{C_{lower}N_{lower}+C_{upper}N_{upper}}{V_{total}}$ ~ $0.99 ; $\frac{N_s C_{upper} N_{mprl}}{V_{design}}$ ~ $1.44



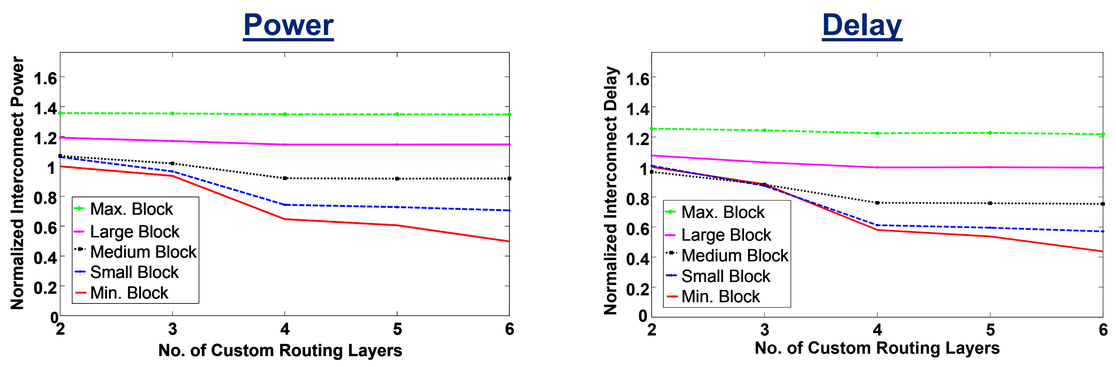
Key Assumptions
- 45nm Maskset Cost: $2.5M
- Total Volume: 2 M
- Per-design Volume: 100k
- Design Re-spins: 1

Chips can be 2-4x Bigger using only 2 Custom Layers

4. CAD Flow

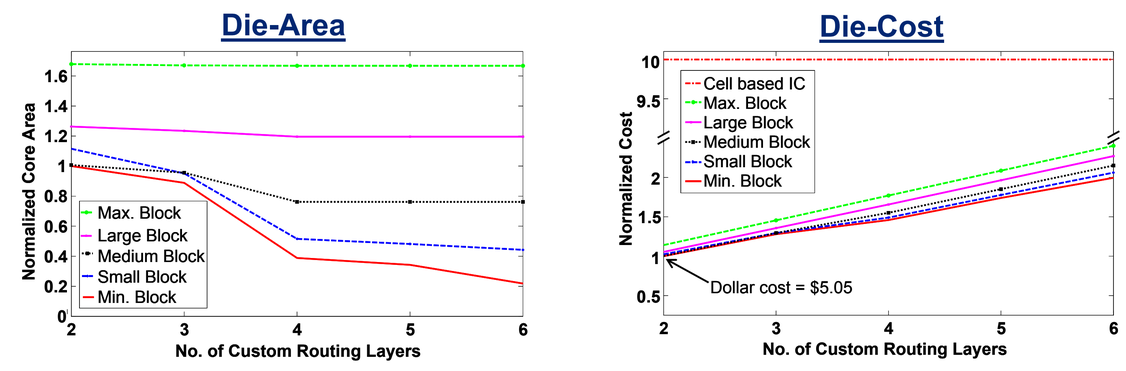


5. Power and Delay Trends



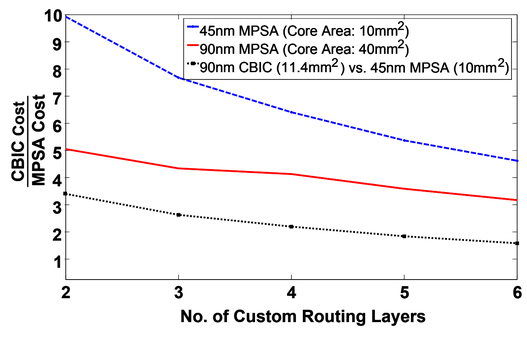
Sparse Layouts: 2 Custom Layers are Good Enough
Dense Layouts: 4 Custom Layers are Good Enough

6. Area and Cost Trends



Area Savings of More Layers != Cost Savings

MPSA vs CBIC



ASICs 2-10x More Expensive than Structured ASICs

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