REAL TIME DISTRIBUTED NETWORK SIMULATION WITH PC CLUSTERS

by
JORGE ARIEL HOLLMAN

Ingeniero Industrial, Orientación Eléctrica,
Universidad Nacional del Comahue, Argentina, 1996

A THESIS SUBMITTED IN PARTIAL FULFILLMENT OF

THE REQUIREMENTS FOR THE DEGREE OF

MASTER of APPLIED SCIENCE

in

THE FACULTY OF GRADUATE STUDIES

DEPARTMENT OF ELECTRICAL ENGINEERING
of the
UNIVERSITY of BRITISH COLUMBIA

We accept this thesis as conforming to the required standard

Ph.D. J.R. Martí, Supervisor ______________________
Ph.D. H.W. Dommel, Reader ______________________
Ph.D. W. Dunford, Head's Nominee & Chair______________________

The University of British Columbia

December 1999

Abstract

REAL TIME DISTRIBUTED NETWORK SIMULATION WITH PC CLUSTERS

by

Elec. Eng. Jorge Ariel Hollman

MASTER of APPLIED SCIENCE

University of British Columbia, Canada

Professor Ph.D. J. R. Martí, Chair

This work presents a new architecture layout to perform real time network simulations distributed among multiple IBM[1]-compatible desktop computers. A network simulation with a PC cluster scheme can successfully cope with the size of growing power systems and fast transient studies. A powerful product has been developed using off-the-shelf Pentium II 400 Mhz personal workstations with a commercially available real-time operating system, standard I/O interfaces, a multimachine scheme and the RTNS[2] real-time power system simulation software as core solver. Models based on the standard tool worldwide for power systems transients simulations, the EMTP[3] program [1],[2], and improved ones for real time performance assure accurate simulation results. Taking advantage of the hardware and software characteristic of the designed simulator, fast and accurate simulations can be executed in a very portable, efficient and economic platform,

[1] International Business Machines Corporation

[2] Real Time Network Simulator

[3] Electromagnetic Transients Program

placing the presented simulator in a better competitive position than expensive TNA's[1] or supercomputer simulator systems.

[1] Transient Network Analyzer

REAL TIME DISTRIBUTED NETWORK SIMULATION WITH PC CLUSTERS

Table of Contents

List of Tables

CHAPTER 1 INTRODUCTION

CHAPTER 2 REAL-TIME DISTRIBUTED NETWORK SIMULATOR ARCHITECTURE

CHAPTER 3 I/O INTERFACE CARD IMPLEMENTATION

CHAPTER 4 TEST CASES

CHAPTER 5 CONCLUSIONS AND RECOMMENDATIONS

List of Figures

CHAPTER 1 INTRODUCTION

CHAPTER 2 REAL-TIME DISTRIBUTED NETWORK SIMULATOR ARCHITECTURE

CHAPTER 3 I/O INTERFACE CARD IMPLEMENTATION

CHAPTER 4 TEST CASES

CHAPTER 5 CONCLUSIONS AND RECOMMENDATIONS

Acknowledgments

I would like to express my gratefulness for the continuous support I received from my family, sponsorship and the UBC power group members, without whom this thesis would not have been possible. I specially would like to thank:

-My beloved wife, Sandra and my daughter Rocío Belén, for their love and unconditional support. They are the light and joy of my life.

-My parents, Esteban Antonio and María del Carmen, for their love and wisdom.

-Ph.D. J. R. Martí, for his guidance and continuous support; for deeply sharing his knowledge; for teaching me the fundamentals of network discretizations; and for trusting me and encouraging me in this work.

-Ph.D. H. W. Dommel, for sharing freely and deeply his knowledge in every possible occasion.

-FUNDACIÓN Y.P.F. for its financial support for the completion of this work.

-M.A.Sc. L. Linares for sharing and teaching me the secrets of highly efficient programming for real-time power system simulation, and M.A.Sc. J. Calviño-Fraga, for sharing with me his extensive knowledge of real-time hardware systems. For their friendship and for their unconditional support.

Jorge Ariel Hollman

To Sandra and Rocío

1 INTRODUCTION

1.1 Previous Work

The present thesis purports to describe the development of a PC cluster for a real-time power system simulator.

The need to achieve real-time simulation for fast power system transients using a distributed solver architecture stems from the fact that simulations performed in a single computer for a given step size can deal only with a natural maximum number of power systems nodes. Unless more sophisticated solver algorithms or faster hardware are developed, this size limit can be a severe restriction. A solution to this problem is presented in this thesis. This solution is based on the concept of mapping a network of inexpensive PC's (PC cluster) to the particular characteristics of the power system solution network.

Day after day the industry and utilities demand more accurate simulators, capable of representing the behavior of larger electrical grids. In addition, it will always be desirable to simulate a given system with a smaller time step since consequently the error introduced in the simulation will also experience a decrease. Even though in our lab a system of 40 nodes can be simulated within 50 microseconds in a Pentium II 400 Mhz, this system cannot be simulated to investigate faster transients than the imposed Nyquist frequency limit according to the chosen time step. A PC cluster simulator proves to be a solution to this limitation.

Today, speed and accuracy are simply not enough. Capability of simulation of bigger systems has become an ultimate goal.

The UBC's RTNS[1] software can achieve real-time performance using a single PC with a defined time step of 50 microseconds for a maximum of 40 nodes and 6 outputs using a Pentium II 400 Mhz.

In an attempt to improve this performance, test case 1 presented in this work simulates a 54 node system in real-time with a time step of 47 microseconds and 6 outputs using two PC Pentium II 400 Mhz. This test case requires 68 microseconds in a single Pentium II 400 Mhz.

Many other research groups around the world are working towards an efficient and economic real-time simulation solution. Among them, UBC power research group plays a leading role since its solution is not only accurate but also fast and inexpensive in comparison to the others.

1.2 Background

There are mainly five well-known research groups working in the field of real-time power system simulators using different approaches. EDF[2] and IREQ[3], have chosen the very expensive and not so portable supercomputer architecture. Manitoba research group has developed a hybrid solution based on a convenient arrangement of either DSP's[4] or

[1] Real-Time Network Simulation

[2] Electricité de France

[3] Hydro Quebec Research Institute

transputers. Mitsubishi started with supercomputers and, after join work with UBC, moved their research to PC's. And last but not least, UBC's research group, was the first one to choose an inexpensive PC solution and achieve real-time performance with this scheme. Recently EDF presented results of a parallel approach based on shared memory architecture. This approach is still based on supercomputers and shows no extra gain in speed in proportion to the number of CPU's in service because the time needed for communication between the CPU's increases with the degree of parallelization [10]. In contrast, the PC cluster architecture proposed in this thesis exhibits a constant communication time for each type of configuration link between the subsystem nodes, independently of the number of node solvers included in the array.

Mitsubishi research group achieved a PC cluster system based on six interconnected machines using a Myricom Myrinet giga-bit network. This approach, as will be explained later in this work, presents a serious performance problem due to its round trip overhead of 15 microseconds [8].

UBC's real-time simulator is based on solid grounds. During the last three decades the software created by H. Dommel [1],[2] —the EMTP[5]— has been steadily recognized and supported by the industry as well as the academic milieu. That support emerged in response to the accuracy and simplicity of the models. All this knowledge evolved in the natural direction within the real-time group to produce a faster network simulator, which indeed is the software known as RTNS [4] created by J. Martí and L. Linares in 1993.

[4] Digital Signal Processing

[5] Electromagnetic Transient Program

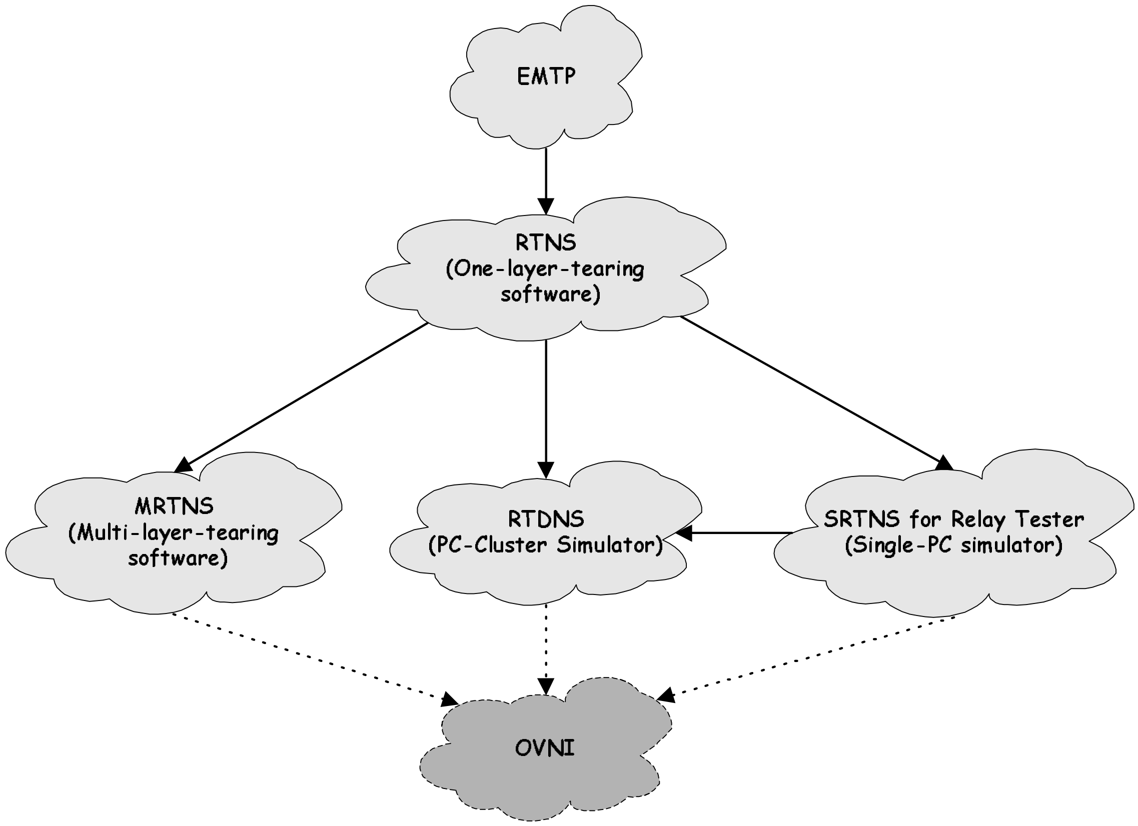


Figure 1-1. *UBC Power system research group past, present & future*

This was the very first PC based real-time network solver. Stemming from this work several other research projects originated, examples of which are the RTNS extensions and hardware implementation for testing Relays [9] developed by J. Calviño Fraga; the Multi-layered tearing solution software developed by L. Linares [3]; and the present work, the RTDNS[6] implementation for multi-PC clusters. See Figure 1-1. These efforts are part of the OVNI[7] project [16] to develop a full system real-time power system simulator.

[6] Real-Time Distributed Network Simulator

[7] Object Virtual Network Integrator

1.3 Paradigm

The main reason for our increased computational efficiency is that UBC’s solution algorithm is structured in the same way as the system it is modelling. In this PC cluster-based layout, dense computational nodes represent the power system substations, while transmission lines connecting substations are represented by simple links to the other dense nodes. See Figure 1-2 on page 6. This segmentation is based on the natural decoupling introduced in the network through the transmission lines. This framework also allows for easy scalability of the computational resources to match the size of the problem. Thus, the PC cluster-based concept perfectly matches the computational paradigm.

Table 1-1 on page 6 presents the obtained results with a single vs. a PC cluster scheme using two computers. The timings were obtained with a non-symmetric node sub-system load, which is not the most efficient situation since the minimum possible time step cannot be used.

As it becomes evident, by using the PC cluster scheme it is feasible for the system size considered to achieve real-time simulation with time steps under 50 miscroseconds, while by using a single computer this would not have been possible.

Table 1-1. *Single PC vs. PC cluster, test case 1*

Tested Configuration	Total Number of nodes simulated in each computer	Number of Outputs	Needed Time to solve the system
Single Pentium II 400 Mhz	**54**	**6**	**62.8 μs**
Two Pentium II 400 Mhz clustered	**30 / 24**	**6**	**46 / 43.6 μs** [a]

[a] For a perfectly symmetric distribution of loads the time step decreases to the minimum. In this benchmark the distribution of load is asymmetric and the time step is imposed by the largest subsystem node.

One crucial aspect of the PC cluster design is its ability to achieve linear scalability. The solution time for each subsystem consists of two parts: the time needed by the computer to solve its own subsystem, and the time needed by the computer to communicate its state to the neighboring computers.Because the communication overhead is independent of the number of machines that make up the cluster, the proposed solution shows linear scalability of system size to be simulated with respect to the number of PC’s used.

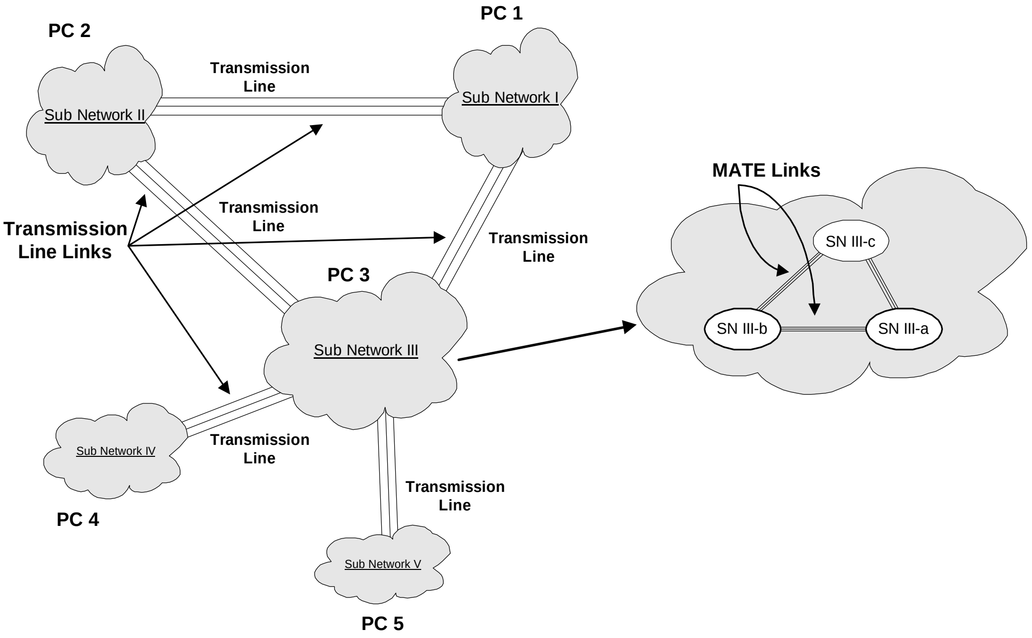


Figure 1-2. Power Network Topology

With the proposed layout, whenever we need to increase the extent of the system representation by one nodal subsystem we only need to add one more computational node to the model, which means just to add another PC to the array.

To achieve real-time performance all the computational processes must be done within the clock time step. Moreover, when real-time performance is required with a PC cluster scheme, in addition to all the computational operations, the communication time between all the elements in the array must be achieved within the clock time step. The proposed solution to cope with this task is based on three fundamental concepts:

- Implementation of double port memory blocks
- Stable and accurate shared-synchronization between the array of computers
- Control of the interrupt requests

The present thesis evolved from previous research work presented by L.Linares and J. Calviño Fraga in their respective M.A.Sc. theses [4],[9].

The core network solver software employed for the *Real-Time Distributed Network Simulator* is the RTNS [4] code originally written by L. Linares. Additional software developed for the RTNS Relay Tester [9] written by J. Calviño Fraga is also used in the present work. New software blocks, a multimachine link line model, and modifications in the original RTNS code were introduced in the present Real-Time Distributed Network Simulator. Finally, a new I/O interface to achieve an efficient and accurate communication between the nodes of the PC cluster was developed.

2 REAL-TIME DISTRIBUTED NETWORK SIMULATOR ARCHITECTURE

2.1 Real-time Simulation under PC Cluster Architecture

Two imperative concepts to consider in a real-time network solution with a multi-machine scheme are the *inherent communication time* and the *synchronization* for each time step.

To achieve real-time performance in more than one machine, solving the system of equations in less than the desired time step is not sufficient. In fact, the transfer of all the necessary data between computers must be done at each time step without violating the imposed time step limit. This situation represents a new challenge, since it means that both the software and the hardware designs must achieve their best performance in order to obtain small solution time steps.

Synchronization is an essential issue in real-time simulations under a PC cluster scheme. A perfect synchronization must be assured in order to present all the outputs scheduled at each tick of the real-time clock, even without knowing the particular performance of each individual computer. An effective source of synchronism must be present in the design to provide the correct clock signals to start the simulation by triggering the network solver processes in all machines at the same time and for all the simulation steps. Further-more, it is also desirable to have the possibility of stopping the simulation in all the components of the multimachine arrangement at any time.

For each real-time clock pulse, adjusted to match the desired time step through the synchronization block, all the computers must:

- Output selected node variables to the A/D card.
- Write needed history terms to the I/O Interface card. Those values will be needed in the neighboring subsystem node to solve for future time steps.
- Read needed history terms from the I/O Interface card. Those data values are provided by the other linked subsystem node.
- Solve the system.

In the case of different computer performances or even in the presence of asymmetrical computational loads, the simulation must allow the slowest subsystem node solver to compute its solution plus transfer the data to the other nodes in less than the time step.

A particular problem present almost in all the I/O interface technologies is related to the latency[1] inherent to the Read/Write process. The architecture designed in this thesis introduces a simple and efficient way to minimize this undesirable overhead[2] time.

[1] The time interval between the instant at which an instruction control unit issues a call for data and the instant at which the transfer of data is started.

[2] The amount of time a computer system spends performing tasks that do not contribute directly to the progress of any user task.

2.2 Network Topology in a PC Cluster

Power Networks can be visualized as separate blocks which are interconnected by transmission lines. See Figure 1-2 on page 6. This network representation proves to be convenient in order to perform a natural and efficient partition of the system to be simulated into several machines, since each individual block is time decoupled by the model of the transmission line.

The MATE[3] concept [16] proposes a general approach to solve a network composed by dense subsystems connected by sparse links as number of computational nodes (e.g., PC's) connected by a link subsystem. The Transmission line link is an example of this general concept and is the one used in this thesis. Future work will further explore the tearing along other types of links.

Under the proposed PC cluster layout, a master unit is in charge of pre-processing the input data, performing the user interface functions, and distributing the solution subsystems among the node solvers (slave computers). This distribution of cases can be accomplished through any standard communications port. For instance, this task can be implemented using either parallel or serial ports for smaller PC cluster arrays and TCP/IP for larger PC cluster ones.

In the present implementation, the master unit is also in charge of setting up the synchronization block through one of the available LPT[4] ports. Each subsystem node solver calculates its part of the network solution while performing the interaction with its neigh-

[3] Multi-Area Thevenin Equivalent.

[4] A port that transfers data one byte at a time, each bit over its own line. Also known as Parallel Port.

bors by using the developed I/O interface card. Under standard PC motherboard configurations, it is possible to interconnect each slave computer with up to two other subsystem nodes.

When interaction with analog equipment is desired, like a relay for instance, it is feasible to include a D/A card, as proposed by J. Calviño-Fraga [9], in the corresponding subsystem node. See Figure 2-2 on page 14.

The master computer can run Windows 95/98/NT while for the subsystem nodes Phar Lap TNT ETS 8.5 [11], a real-time operating system, is chosen.

The highest computational power is required for the subsystem computer nodes, but no other extra peripheral device unit is needed. These nodes can consist of only the CPU, motherboard, floppy disk and RAM memory. To avoid the inclusion of a floppy disk unit in each slave computer a boot PROM[5] in which the real-time operating system is loaded is implemented.

2.3 Integration Rule Accuracy vs. Nyquist Frequency

The Nyquist frequency is the bandwidth of a sampled signal, and is equal to half of the sampling frequency of that signal. In step by step time-domain simulation, the sampled signal should represent a continuous spectral range starting at 0 Hz, the Nyquist frequency is the highest frequency that the time-domain solution will contain.

[5] Programmable read-only memory. A form of nonvolatile memory that is supplied with null contents and is loaded with its contents in the laboratory or in the field. Once programmed, its contents cannot be changed.

$$f_{Ny} = \frac{f_{sample}}{2} = \frac{1}{2.\Delta t}$$

The smaller the integration time step, the higher Nyquist frequency.The associated distortion error introduced by the integration rule increases as the frequency in the simulation gets closer to the Nyquist frequency. For a given frequency in the simulation, the error will decrease if the time step is reduced. See Figure 2-1.

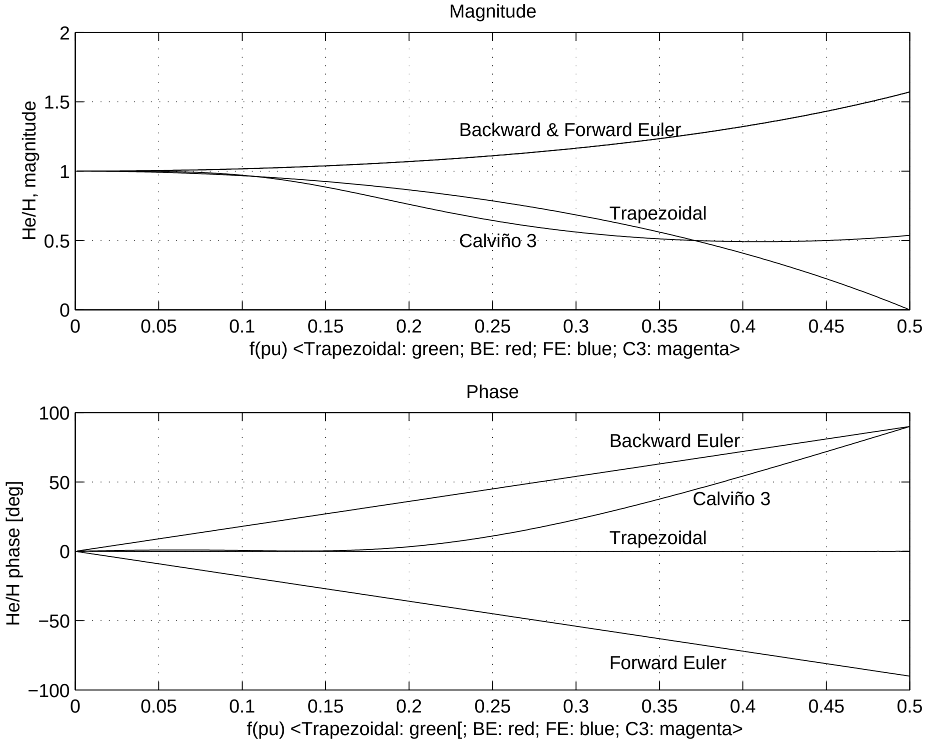


Figure 2-1. *Frequency response of integration rules*

In power system transients simulation it is desirable to obtain an accurate representation of high frequencies when fast transients are applied (e.g. fast switching operations, HVDC[6] converters, TRV[7] studies). Beyond a certain system size, it is not possible to

[6] High-voltage direct-current systems

[7] Transient Recovery Voltage

achieve accurate results, with an acceptable distortion error, unless a faster CPU or a faster solution algorithm is implemented. An alternative solution to this situation is to simulate the power system with a PC cluster architecture, which speeds up the global solution.

For instance, test case 1 simulated in a single Pentium II 400 Mhz can not achieve real-time for a distortion error less than 3% at a frequency of 2kHz, but if the same system is simulated with a PC cluster, real-time can be achieve with the desired accuracy.

2.4 Input/Output Interface Port Selection

To achieve real-time performance using the PC cluster scheme with a time step of 50 microseconds with 6 outputs per subsystem node, and solving the network system with RTNS[8], a maximum communication time of 0.45 microseconds per byte transferred is imposed. This limit permits keeping the maximum distortion error introduced by the integration rule under 3%, as well as the use of three phase single and double circuit line links between subsystem nodes. The necessary bandwidth is determined by the amount of data to be transferred between solver nodes.

An input/output standard interface such as a parallel port in its configuration EPP[9] and ECP[10], including the outstanding PCI-EPP/ECP interface technology, is not fast enough for the requirements of RTNS with a multimachine scheme.

Certain input/output standard interfaces offer high transfer rates. However, these transfer rates are valid only for very large memory blocks. This results from the fact that

[8] Real-time Network Simulator

[9] Enhanced Parallel Port

[10] Extended Capabilities Port

they are meant for video, massive storage devices, or the video-conference applications in which great volumes of data need to be exchanged. Examples of the above I/O standards are PCI[11], SCSI[12] and AGP[13].

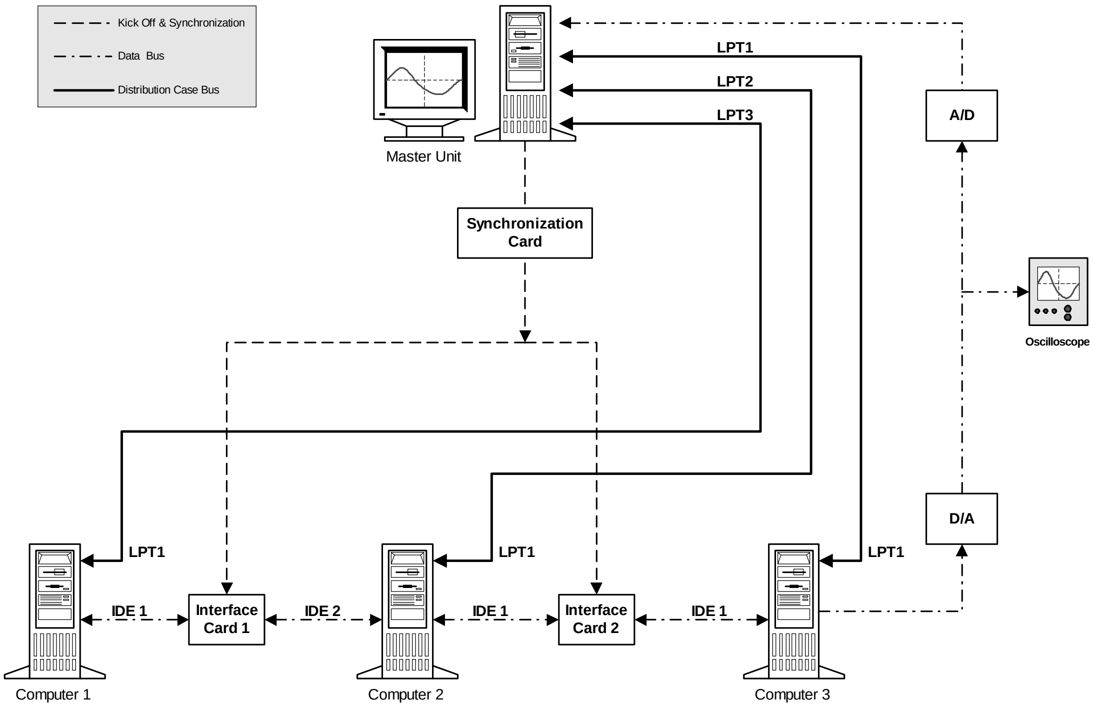


Figure 2-2. *Proposed Multimachine solution architecture*

In applications like RTNS, the needs are different since instead of transferring large amounts of interchanged data the objective is to transfer at high transfer speed small memory blocks. In order to complete each transfer cycle even in the case of small-sized blocks these massive I/O standard interfaces consume much more time than the allowed

[11] Personal Computer Interface

[12] Small Computer System Interface

[13] Accelerated Graphics Port

time step size for most of the power simulation cases. Consequently, these devices do not meet the real-time power system simulation requirements.

Although the SCSI I/O interface seems more attractive than IDE because of its capability of transferring 32 data bits at each hand shake, it is not entirely suitable for our application since it is not directly connected to the CPU bus. There is no point in using a more expensive SCSI based system when the lower-cost ATA/IDE interface will do a better job. The IDE I/O interface is directly connected to the computer bus and it is not necessary to use an extra driver or card to write or read the desired data. Not only is the IDE interface faster and more economical, but also the system is not tied to any third part vendor or manufacturer of the driver as in the SCSI alternative.

All standard PC computers have at least two IDE ports in their motherboard. Each of them can address two devices. Some of our measured data transfer rates for the EPP/ECP, PCI-EPP/ECP and IDE I/O interfaces are shown in Table 3-1 on page 21.

Special consideration is given to communication networks like the costly Myricom Myrinet networks chosen by some research groups such as Mitsubishi. These type of networks are not suitable for our real-time network requirements. Even though they can achieve transfer rates between 78 MBytes/sec and 120 MBytes/sec, their roundtrip time is remarkably large, from 15 to 25 microseconds. For instance, using a Myricom Myrinet network the necessary time to transfer 4 KBytes is 25.6 microseconds while with the pin-down option the roundtrip time is increased up to 47 microseconds [7], where the pin-down[14] cost depends on processors and operating systems. For smaller memory blocks the latency is

[14] *User virtual memory must be copy to a physical memory location before the message is sent or received.*

more important and the consequent bandwidth smaller. These type of networks are designed to transfer extensive amount of data but are not fast enough to reconfigure themselves in a few microseconds for repetitive small size data block transfers as required in our problem of power system transients simulation.

For all the above mentioned reasons, the IDE I/O interface was chosen in the present thesis to interconnect the subsystem computers.

2.5 I/O Interface Latency

Latency is understood as the time required to read from or write to a storage device after the proper controls and addresses have been applied. This overhead time is also present when data transfer between computers is performed. In real-time applications with time steps in the order of microseconds, the lack of care for this accessing time can be the difference between the success of the communication process or its failure.

The communication channel cannot be used until the initialization process finishes and the hardware-software implementation needs a rather complicated synchronization procedure in order to avoid simultaneous access requests from the communicating computers. For example, in the case of two computers that finish their step calculation at the same time, they need to wait twice the necessary data transfer time before they complete their cycle and start the next time step calculation, this in addition to the time required to send and receive the communication request acknowledge.

An effective way to reduce the latency problem as well as to provide the communication system with a pseudo simultaneous bidirectional response is through the use of a double-port memory array between computers. *Dual Port Static Random Access Memories* allow two independent devices to have synchronous access to the same memory. Both devices can then communicate with each other by passing data through the common memory. A DPM[15] has two sets of addresses, data and read/write signals, each of which access the same set of memory cells. Each set of memory controls can independently and simultaneously read any word in memory including the case where both sides are accessing the same memory location at the same time. See Figure 3-5 on page 26.

The I/O interface card developed in this work uses a DPM configuration with two pages, where one of the pages is dedicated to write the data and the other one to read it.

Since the memory is transparent to both computers, a re-direction to the appropriate page for each computer can be implemented with suitable hardware programming. See Figure 2-3 on page 18. In that way the data transfer can be done simultaneously for both machines thus reducing the latency communication time even to a negligible value. During the real-time simulation, both subsystem nodes perform the writing and reading process at the same time. This feature permits the code for any of the subsystem nodes to be transparent to the process, without having to include any special waiting cycle to perform the data transfer.

In the proposed implementation, the latency problem is considerably reduced because when either of the computers needs to read o write data, the memory is always available. The access time to the double port memory is 35 nanoseconds for the chosen IDT

[15] Dual Port Memory

double memory chip [12], and the inherent IDE port round trip latency using PIO[16] mode 2 is of approximately 3 microseconds for a memory block of 48 Bytes.

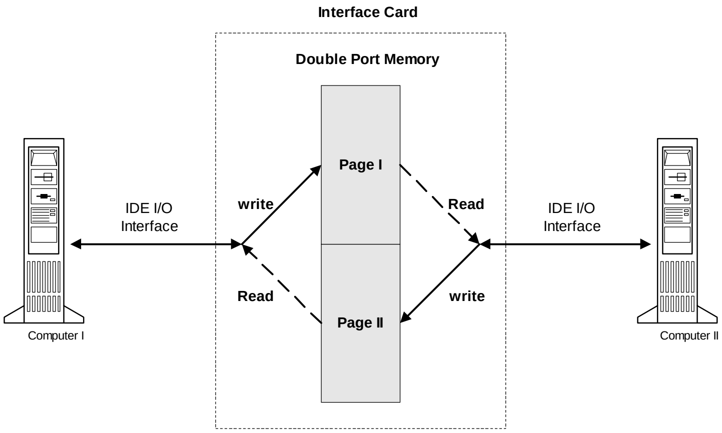


Figure 2-3. *Double Port Memory functionality*

Some motherboards implement a common PCI bus on top of which the IDE bus is running. To make compatible the IDE peripheral devices with the PCI bus speed, the IDE signals are controlled with the granularity of the PCI clock. For instance a data port compatible IDE transaction type takes a total of 25 PCI clock pulses [15]. Under this situation an extra overhead is introduced since the PCI latency must be considered. The options to improve the IDE transfer performance are:

- use the most appropriate PIO mode.
- choose a different system architecture, such as Intel 810e chipset, which allows the IDE port to access directly a faster system bus.
- configure the PCI latency cycles to a faster transfer mode.

[16] Programmed Input/Output

There are five PIO IDE timing modes: 0, 1, 2, 3, and 4. Modes 0 through 4 provide successively increased performance.

IDE data port transaction latency consists of start-up latency, cycle latency, and shutdown latency. Start-up latency is incurred when a PCI master cycle targeting the IDE data port is decoded and the data address and chip select lines are not set up. Start-up latency provides the setup time for the data address and chip select lines prior to assertion of the read and write strobes.

Cycle latency consists of the I/O command strobe assertion length and recovery time. Recovery time is provided so that transactions may occur back-to-back on the IDE interface (without incurring start-up and shutdown latency) without violating minimum cycle periods for the IDE interface. The command strobe assertion width for the enhanced timing mode is selected by the IDETIM Register and may be set to 2, 3, 4, or 5 PCI clocks. The recovery time is selected by the IDETIM Register and may be set to 1, 2, 3, or 4 PCI clocks.

If IORDY is asserted when the initial sample point is reached, no wait states are added to the command strobe assertion length. If IORDY is negated when the initial sample point is reached, additional wait states are added. Since the rising edge of IORDY must be synchronized, at least two additional PCI clocks are added.

Table 2-1. *IDE Transaction timings (PCI clock)*[a]

IDE Transaction Type	Start-up Latency	ISP	RCT	Shutdown Latency
No-Data Port compatible	**4**	**11**	**22**	**2**
Data Port compatible	**3**	**6**	**14**	**2**
Fast Timing Mode	**2**	**2-5**	**1-4**	**2**

[a] for instance with a PCI bus of 33 Mhz, each PCI clock takes 30 nanoseconds.

3 I/O INTERFACE CARD IMPLEMENTATION

3.1 Input/Output Interface Card

The IDE port was chosen for several reasons: to achieve portability, to ensure the necessary transfer rate, and to follow the policy of using only off-the-shell computer components. Since the IDE port is available in all motherboards at the present time it makes a perfect choice from the portability point of view, also allowing to maintain a low design cost.

Previously to the selection of the IDE port, the parallel port was tested applying the same block design, but the obtained maximum transfer rates were below or near the imposed limit for the real-time requirements when standard LPT and fast PCI LPT ports were tested. This is shown in Table 3-1 on page 21.

Transfer rates between 0.23 and 0.32 μs/Byte were achieved using the adopted approach in almost every standard Pentium Pro and Pentium II PCs, giving an extraordinary portability to the design. Obtained rates depends on the selected operating mode and the system bus architecture.

A minimum time step of 50 μs for the test cases was chosen in order to keep the maximum distortion error under 3% for the trapezoidal integration rule representing frequencies up to 2 kHz. This constraint places the desired transfer rate in ranges of less than

0.45 µs/byte for the case without further data optimization, and in a smaller transfer rate for the case with data optimization.

Table 3-1. *Data Transfer Rates*

I/O Interface	**Dell Pentium MMX 233 Mhz**[a]	**Bus Width [bits]**	**Time needed for 3 phase *Transmission Line***
EPP/ECP (Parallel)	**2.4 µs/Byte** **[0.416 MB/sec]**	**8**	**57.6 µs**
PCI - EPP/ECP (Parallel)	**1 µs/Byte** **[1 MB/sec]**	**8**	**24 µs**
IDE	**0.3 µs/Byte** **[3.3 MB/sec]**	**16**	**7.2 µs**

[a] The CPU speed does not impose a great difference in the port transfer timings.

The feasible number of line links to be connected in the PC cluster scheme between subsystem nodes depends on four variables:

- Size of the subsystem
- CPU speed
- Number of Outputs
- Symmetry of the distribution of loads among the subsystem nodes

A more flexible link connection scheme is obtained when the following conditions are met: A faster subsystem node CPU, a smaller number of outputs, and a smaller size of the case system loaded in each CPU node. The presence of a perfect symmetry of computational loads guarantees the maximum gain of speed of the cluster array. For instance, using a Pentium II 400 Mhz, three outputs, loading each subsystem node with a case of size

30 nodes, and a time step of 50 microseconds, it is possible to implement the following configuration of links:

- Two 3 phase circuits: communication of the subsystem node to other two subsystem nodes. Figure 3-1, scheme I.
- One 3 phase Double circuit: communication to another subsystem node. Figure 3-1, scheme II.

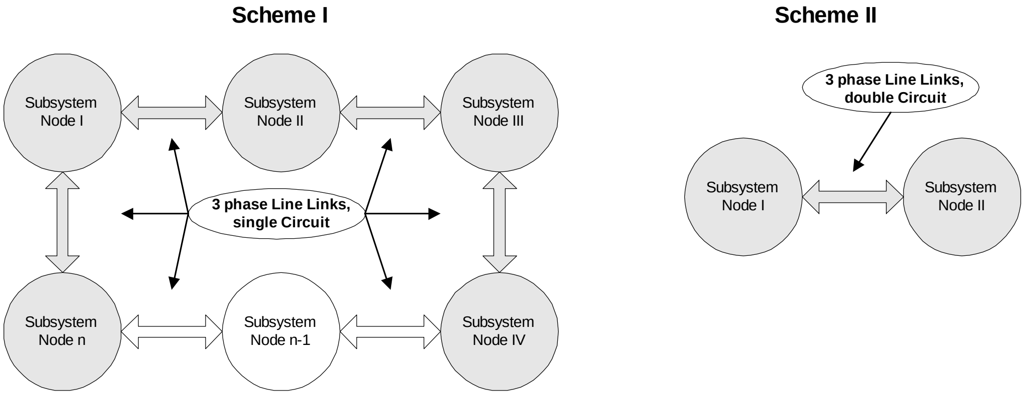


Figure 3-1. *Connectivity alternatives with a PII 400 Mhz*

Just by upgrading the CPU from a Pentium II 400 Mhz to a Pentium III 600 Mhz, within a time step of 50 microseconds, and keeping the previous setting of three outputs and a 24 node subsystem load, the schemes shown in Figure 3-2 on page 23 are feasible of implementation.

The inherent flexibility of the approach is based on the simplicity of the communication concept and on the fixed communication time characteristic for a given subsystem node connectivity layout which is independent of the number of computers added to the PC cluster array.

Better performances can be achieved with the implementation of data optimization algorithms, such as delta modulation or data compression processes.

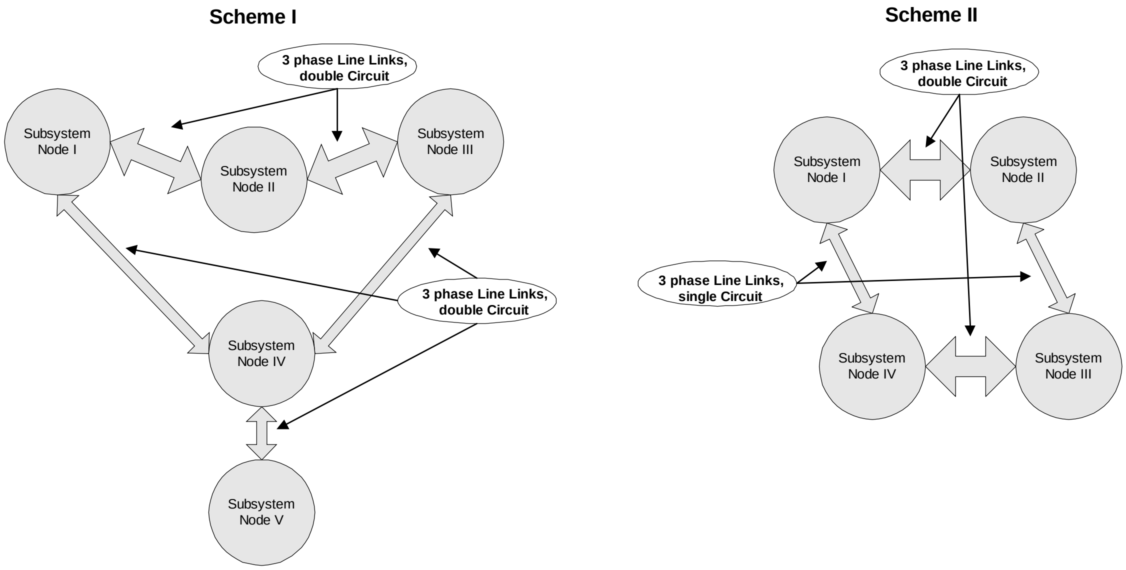


Figure 3-2. *Connectivity alternatives with a PIII 600 Mhz*

3.2 Design Process and Prototype Implementation

Three CAD tools were used to produce the prototype the hardware interface card implementation shown in Figure 3-3 on page 24, and Figure 3-4 on page 24. During the period of design and evaluation of the individual groupal blocks, both OrCad and an experimental protoboard were used. See Figure I-1 on page 60. Once the final prototype version presented in this thesis was defined, OrCad and Tango were run to obtain the translation of the schematic into the Netlist and the Printed Circuit Board version respectively. Appendix I includes illustrations of the circuit schematics and PCB[1] files.

[1] Printed Circuit Board

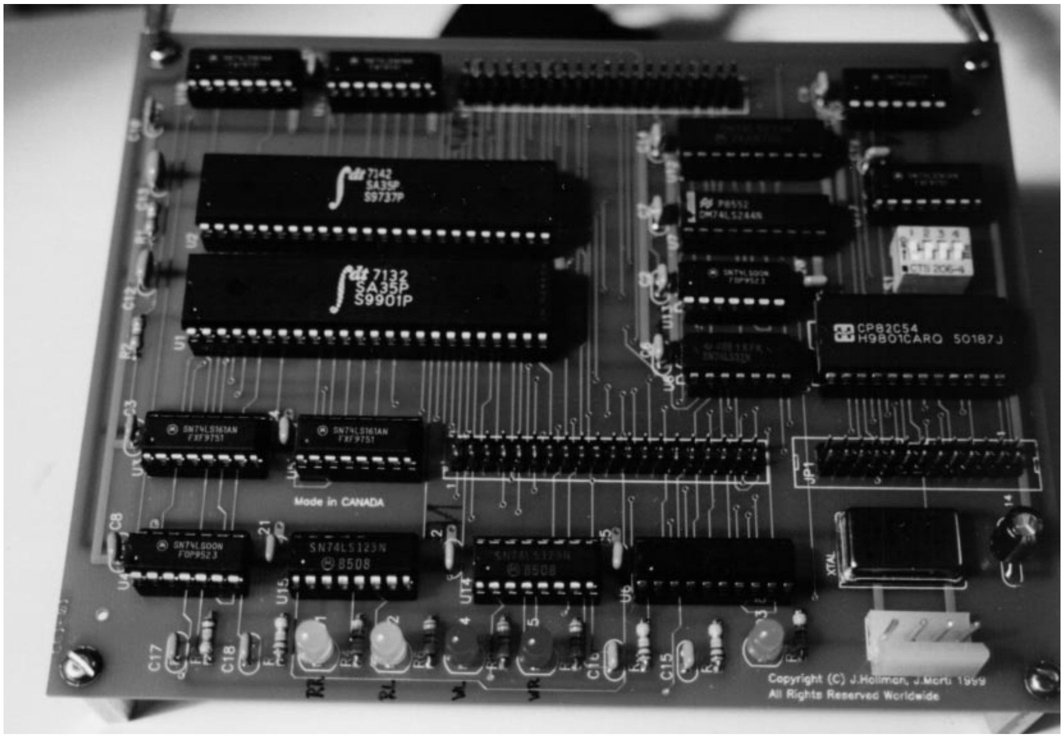


Figure 3-3. *Picture of the I/O interface card, component side*

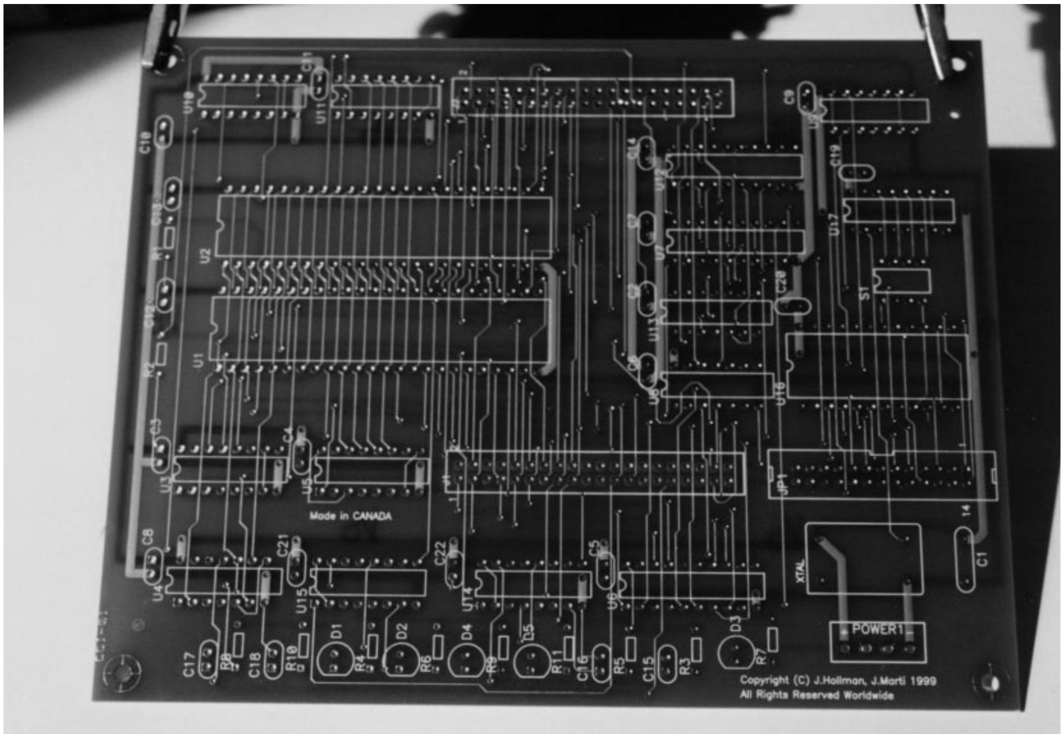

U1
U2
U3
U4
U5
U14
U15
U16
U17
JP1
S1
XTAL
POWER1
Made in CANADA
Copyright (C) J.Hollman, J.Marti 1999
All Rights Reserved Worldwide

Figure 3-4. *Picture of the I/O interface card, bottom side*

3.3 Double Port Memory Block

The DPM[2] block is the central element in the present I/O interface card. This block is in charge of storing and transferring data between the node subsystems. Each subsystem writes and reads data from different memory pages. See Figure 2-3 on page 18. The available memory resource for each subsystem node using the chosen IDT7132 [12] is 16K[3] (2K x 16 Bit). For instance, each page can address 512 memory cells.

The IDT7132/7142, the master and the slave DPM, provides two ports with separate controls, addresses, and I/O pins that permit independent access to read or write to any location in the DPM. Since the implemented software for both subsystem nodes writes and reads to/from the DPM in different memory pages, and since both simulations are perfectly synchronized through the external synchronization block, there is no possibility for simultaneous access conflicts in the DPM.

For every time step during the data transfer, subsystem node I writes the data into memory page 1, while subsystem node II writes it into memory page II. Next, subsystem node I will read the data from page II while subsystem node II will read it from page I.

To know which memory cell should be addressed a hardware counter is used every time the memory is accessed. The counter is implemented through a pair of synchronous binary 4 bit counters, such as the 74LS161. When the process of writing data is started at every time step, the counter is reset to the first position in page I on one side of the memory array and in the other half of the memory it is reset to the first position in page II. This

[2] Dual Port Memory

[3] Applying Width Expansion with the IDT7142 “slave” DPM.

counter is incremented after each memory cell is filled. Once this process is accomplished, the counters are reset again to the correct values in order to read from the proper pages.

The DPM is available to each subsystem node at any moment, and it can be accessed simultaneously. In this implementation the simultaneous access condition is limited to different pages and access is not allowed to an individual memory cell.

To clean up the signals and assure a proper functionality, all the DPM control lines — Chip select, Write, Read, and Busy — are passed through an octal D-type flip flop. The chosen 74LS273 successfully copes with this task. See Figure I-3 on page 62.

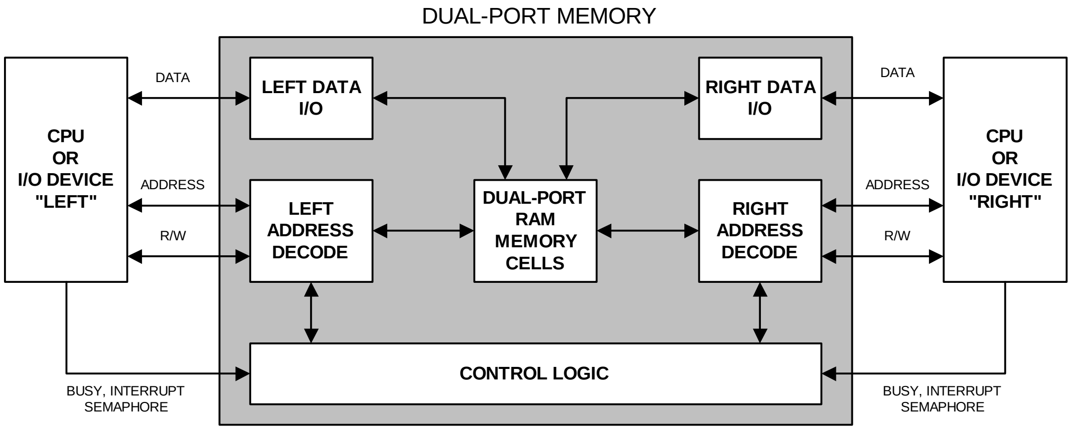


Figure 3-5. *Dual Port Memory Block Diagram*

DPMs can be combined to form large dual port memories using master and slave memory components. In the design described here, a set of two DPMs is used in each I/O Interface card in order to obtain an array of 2K x 16 bits memory blocks. See Figure 3-6 on page 27. This situation is strikingly useful because since the IDE port is used, 16 bits can be written or read at any handshake without any further delay. Even though a depth expansion with this type of devices is feasible, for the present applications it is not necessary to incorporate this option in the design.

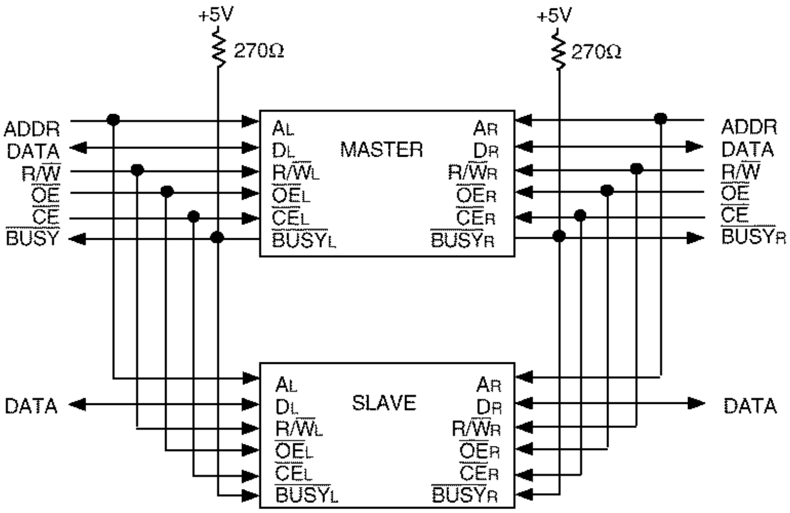


Figure 3-6. *Memory width Expansion*

3.4 Synchronization Block

In real-time simulation all the necessary operations must be completed within the adopted time step. Moreover, as the size of the network assigned to each machine can be different as well as the capability of each computer to perform the subnetwork calculation, it is desirable to count with an independent synchronization source. When the subsystems calcutations are finished, this source is in charge of triggering a signal to all the cluster computers so that they start each individual subsystem calculation for the upcoming time step synchronically with the real time clock.

The simulation program must only verify that the slowest computer in the system is capable of solving the system and sending the data within the time step. Then all the other computers will follow the slowest one or the one with more calculation load.

Another function incorporated into the synchronization block is the start-off signal. This signal allows the user to start and interrupt the simulation in all the machines simultaneously.

The main advantage of using an external source of time is that it can be selected with the appropriate accuracy and it can be easily shared by all the computers in the parallel array. In the present work, a Programmable Internal Interval Timer CHMOS was selected to provide the external real-time clock, where the resolution can be expressed as follows:

$$\delta = \frac{1}{\text{frequency}}$$

Since the first IBM PC based in the 8088 microprocessor appeared, and up to current high performance Pentium based PCs, these type of counters have been available and have remained unchanged. For the earlier PCs the 82C53 was first used, and later it was replaced by the 82C54 which exhibits an improved and backward compatible design.

Six programmable timer modes allow the 82C54 to be used for several applications (e.g., as a counter, as an elapsed time indicator, or as a programmable one-shot). See Table 3-2 on page 29. The selected working mode for the I/O card design presented in this work is mode 3, a square wave generator.

The alternative of using an internal source of time provided by each subsystem node is not suitable for PC cluster layouts, since it makes the synchronization among the slave nodes much more difficult, and it also increases the complexity of the communications.

Table 3-2. *82C54 Operation Modes*

MODE 0	INTERRUPT ON TERMINAL COUNT
MODE 1	HARDWARE RETRIGGERABLE ONE-SHOT
MODE 2	RATE GENERATOR
MODE 3	SQUARE WAVE MODE
MODE 4	SOFTWARE TRIGGERED STROBE
MODE 5	HARDWARE TRIGGERED STROBE

The real-time source is configured through one of the parallel ports available in the master unit. During the process of configuration of the synchronization block the interrupts are disabled. An associated error will be present in the delta t, since the hardware time step is obtained trough an integer value programmed into the counter when the desired time step is not an integer multiplier of delta. However, the error introduced is not relevant (e.g. +/- 0.0625 nano seconds). Another error of around 25 ppm[4]/ºC is present in the real-time clock introduced by the crystal. The real-time clock resolution for the chosen crystal is:

$$\delta = \left(\frac{16\mathrm{Mhz}}{2}\right)^{-1} = 0.125\mathrm{ns}$$

Programming of the 82C54 is available to the user through the simulator's GUI[5], since it is necessary to reprogram the external timing source when a new delta t is chosen

[4] parts per million.

[5] Graphical User Interface

for a simulation. The Control of the Synchronization is implemented in the master unit computer.

The 82C54 can be fed with a crystal of a frequency of up to 10 Mhz, achieving a maximum resolution of 100 nanoseconds for the external timing source. The designed circuit allows flexibility since higher frequency crystal oscillators can be also used through a convenient frequency divider. For instance, with a crystal oscillator of 20 Mhz with a division factor of 2, a final precision of 100 nanoseconds is obtained. This feature is achieved through a Synchronous 4 BIT counter, the 74LS161. Figure I-3 on page 62.

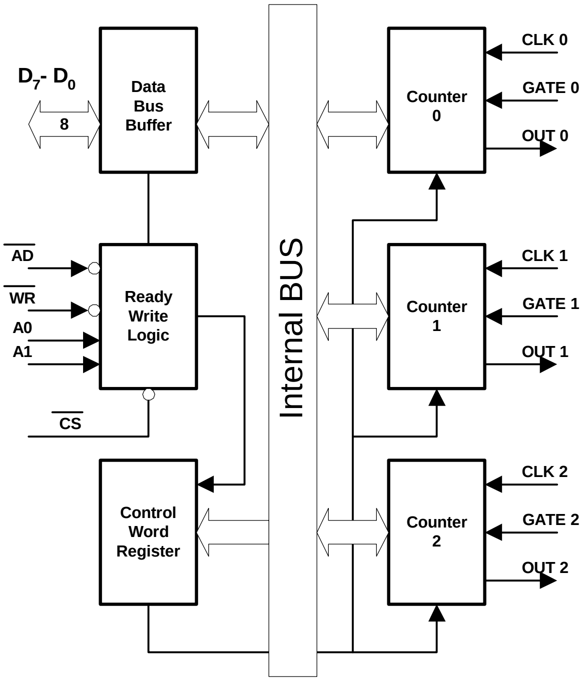


Figure 3-7. *82C54 CHMOS Programmable Internal Interval Timer*

When a control word is written to one of the counters, all control logic is immediately reset and the output goes to a known initial state.

The 82C54 counters are programmed by writing a control word and then an initial count. The control words are written into the control word register, which is selected when pins A1 & A0 are set to 1, and the control itself specifies which counter is being programmed.

Each of the three timers included in the 82C54 have a resolution of 16 bits, one in 65536 multiplies of the input frequency period.

After writing a control word and initial count, the counter will be loaded on the next clock pulse. This allows the counter to be synchronized by software. The control word format is as follows:

Control Word Format

A1, A0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ =0

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC - Select Counter :

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command

RW - Read/Write :

RW1	RW0	
0	0	Counter Latch Command
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first then most significant byte

M - Mode :

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
x	1	0	Mode 2
X	1	1	Mode 3
X	0	0	Mode 4
1	0	1	Mode 5

BCD :

0	Binary counter 16 bits
1	Binary Coded Decimal (BCD) cunter

The following is part of the C code to accomplish the 82C54 programming:

```
// Available LPT Ports
int Base [3] = { 0x338, 0x378 , 0x278 };
int Port;
unsigened char timer_low, timer_high;
double deltaT;
// 82C54 Output Format
#define MODE2 0x34         //Mode 2, Pulse
#define MODE3 0x36         //Mode 3, Square Wave
#define Output 2
#define Input 1
#define Data 0
#define ko 4

DisableInterrupts ();

//Setup the 'hardware' deltat
timer_value = RoundRealToNearestInteger (deltaT*CLKIN);
timer_low    = timer_value%0x100;
timer_high   = timer_value/0x100;

//82C54 Selection Mode
outp ( Base [Port] + Output , 0 | ko );
outp ( Base [Port] + Data  , MODE3 );
outp ( Base [Port] + Output , 1 | ko );
outp ( Base [Port] + Output , 0 | ko );

//Divider Settings 8254
//Low Byte
outp ( Base [Port] + Output , 0xA | ko );
outp ( Base [Port] + Data  , timer_low );
outp ( Base [Port] + Output , 0xB | ko );
outp ( Base [Port] + Output , 0xA | ko );
//High Byte
outp ( Base [Port] + Output , 0xA | ko );
outp ( Base [Port] + Data  , timer_high );
outp ( Base [Port] + Output , 0xB | ko );
outp ( Base [Port] + Output , 0xA | ko );

EnableInterrupts ();
```

3.5 Process Panel Indicator Block

To obtain an external visualization of the transfer data process status, two leds, which are used to indicate the active read or write processes, are added to each half of the design. This function is implemented with four retriggerable monostable multivibrators, such as the 74LS123. Since the transfer process is too fast, a small time delay is introduced to the monostables multivibrators to assure that their status can be easily visualized.

3.6 Digital/Analog & Analog/Digital Cards

In order to access the analog outputs and digital inputs of the simulation computer, the monitoring computer requires the appropriate data acquisition hardware. The selected hardware is a multi I/O board from National Instruments, the AT-MIO-16 [17]. This board provides 16 analog inputs with a resolution of 12 bits (11 bits + sign). The drivers provided by National Instruments are used to access the AT-MIO-16.

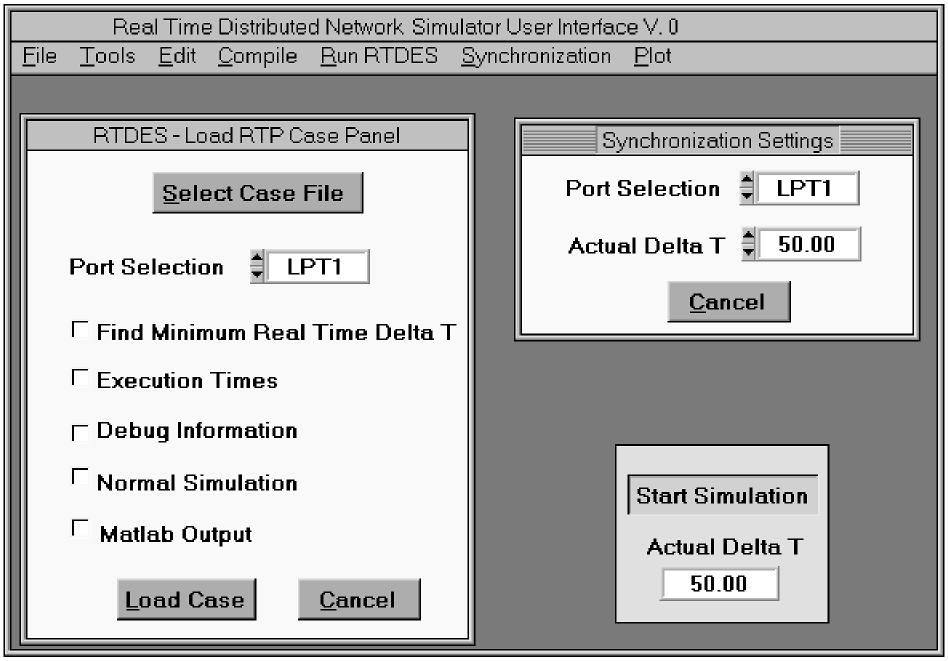
3.7 Graphical User Interface

To cope with the task of setting up and running the study cases with the real-time distributed network simulator, a basic GUI was implemented. This GUI was developed using the CVI software tool [13] from National Instruments. The main functions included in the GUI are the following:

- Synchronization block set up
- Real-Time Distributed Network Simulator cases Edition and Compilation
- Simulation condition set up
- Link to Software Tools, such as Matlab, Schematic editor, Microtran and WinPlot.
- Cases Load and Distribution among the Pc cluster array.

- Start/Stop simulation control

The introduced GUI is a beta implementation, and it merely intends to simplify the testing and researching processes, but it could serve as a base element to develop a more flexible and powerful GUI user interface for future RTDNS versions. Figure 3-8 on page 34 shows a snapshot of the above mentioned interface.



Port Selection LPT1

☐ Find Minimum Real Time Delta T

☐ Execution Times

☐ Debug Information

☐ Normal Simulation

☐ Matlab Output

Port Selection LPT1

Actual Delta T 50.00

Actual Delta T 50.00

Figure 3-8. *Snapshot of the implemented Control GUI*

3.8 Link Line Block

The link line block is a lossless transmission line model implementation with the losses lumped at the line ends. The decoupling provided by the lossles line makes possible the solution of the network using a PC cluster array. The lossless transmission model is clearly explained by Dommel and Martí in [2], [14] and can be represented by the following equations in the modal domain:

$$H_{mi}(t) = 2.G_i \cdot V_{ki}(t-\tau) - H_{ki}(t-\tau)$$

$$H_{ki}(t) = 2.G_i \cdot V_{mi}(t-\tau) - H_{mi}(t-\tau)$$

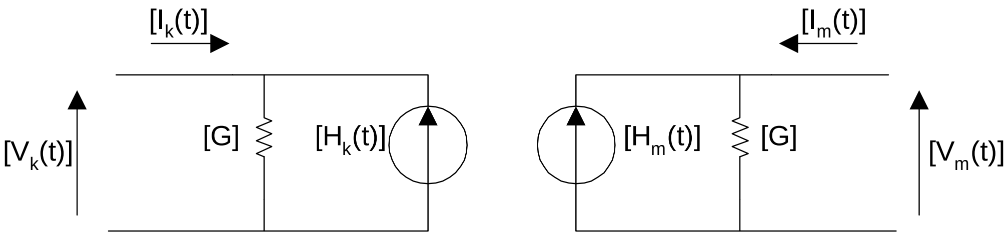


Figure 3-9. *Lossless Transmission Line model in phase domain*

In the model, G_i is the conductance of mode i, τ_i the propagation time of mode i and H_{ki} the modal history value of the considered node. Since the rest of the network is always defined in phase quantities, these modal equations must be transformed to phase quantities to complete the solution at each time step. The connection between modal and phase domain can be graphically represented as follows:

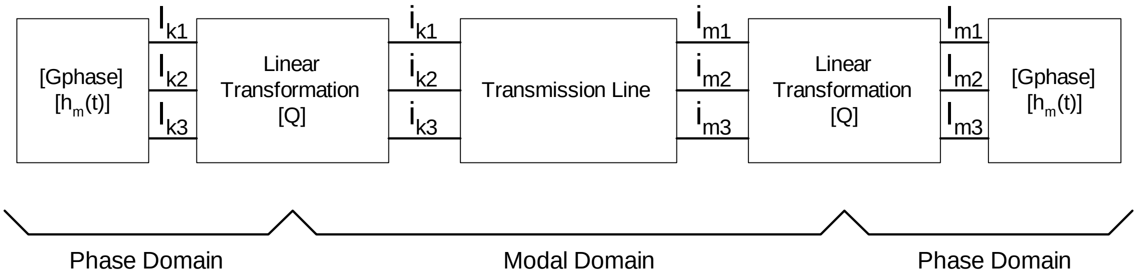


Figure 3-10. *Phase and Modal domain connection for a three phase line*

The modal matrix [G] is pre-calculated and fixed for a given time step. The history terms, both in modal and phase domain, must be re-calculated at each time step. The needed number of history values to remember can be expressed as follows:

$$n = \mathrm{int}\left(\frac{\tau}{\Delta t}\right) + 1$$

To split the calculation of the lossless transmission line between two computational nodes at each time step, three voltages and three voltage history terms need to be transferred. Since the time price inherent to the data transfer is by far more expensive than the computational time, it was important to realize in the implementation that only the voltages at the other end need to be transmitted while the histories can be recalculated at the local node. In that way for a three phase transmission line only three phase voltages are needed to be transferred at each time step. Then each solver node will perform the calculation of an equivalent full line but receiving half of the voltage nodes from the other solver node through the I/O interface card.

The functional diagram of the link line block implementation is shown in Figure 3-11 on page 37.

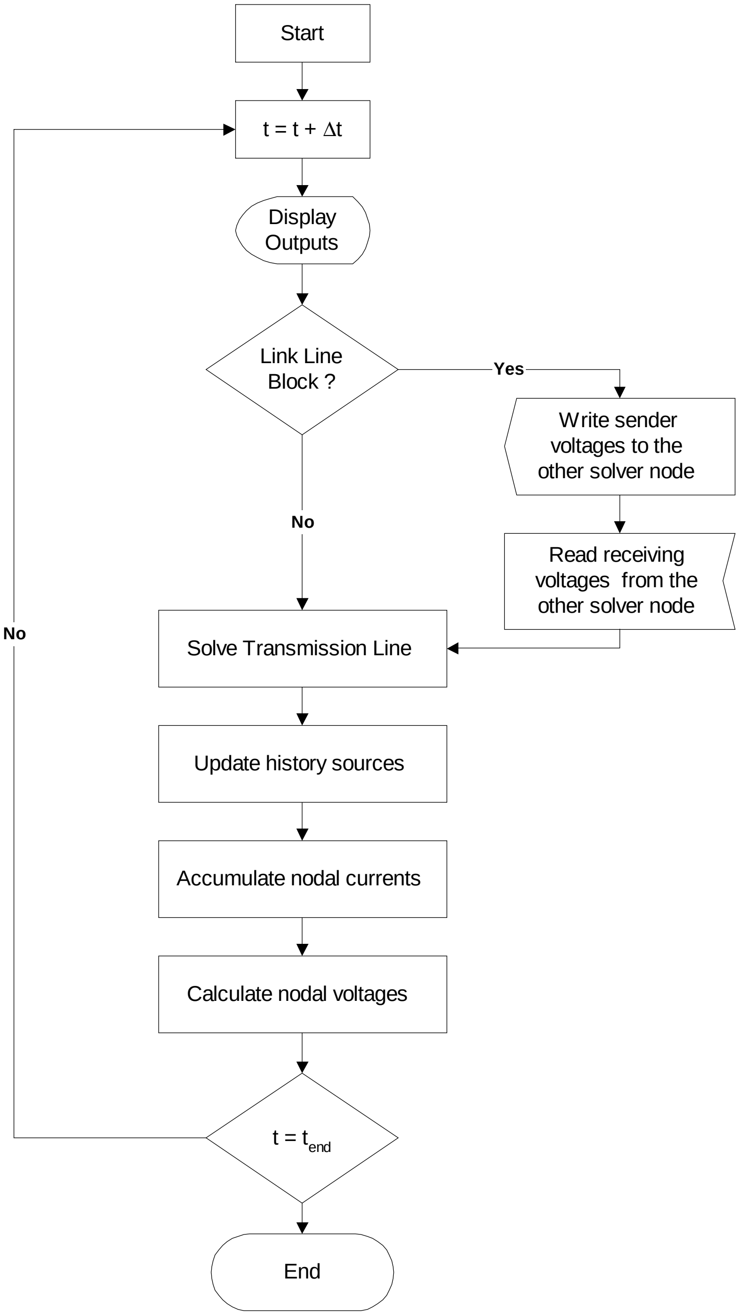


Figure 3-11. *Link line block implementation*

The aim was to implement the link line block making it fully compatible with the RTNS line model as well as with the developed hardware. In this way the user can still distribute the original RTNS cases in the new PC cluster array running RTDNS by only adding the type of line used. For instance, all lines have an extra flag parameter -MmLink- which defines whether the line is used as a multimachine link or is fully solved in a single PC. The same flag is used to identify to which IDE port the link line must be connected. The rest of the transmission line data follows the same structure used by RTNS.

```
...
phases: 6
MmLink: 1
Zc: 987.9 328.4 275.9 222.6 237.2 244.1
...
```

Table 3-3. *MnLink Flag options*

Link Line Options	MmLink Value
Normal Lossless transmission line solved in a single PC	**0**
Lossless transmission line solved in PC cluster array - Link between PC nodes-, connected to IDE port 1	**1**
Lossless transmission line solved in PC cluster array - Link between PC nodes-, connected to IDE port 2	**2**

The following C code shows how the process of reading and writing the data from and to the I/O interface card is implemented.

```
if (line[i].mmlink==1)
{
  outp(IDE0_CS1, 4 | 0x80 );
  ReadMm3phLine ((unsigned short int *)&v1_mm, IDE0_CS0);
  ReadMm3phLine ((unsigned short int *)&v3_mm, IDE0_CS0);
  ReadMm3phLine ((unsigned short int *)&v5_mm, IDE0_CS0);
}
else if (line[i].mmlink==2)
{
  outp(IDE1_CS1, 4 | 0x80 );
  ReadMm3phLine ((unsigned short int *)&v1_mm, IDE1_CS0);
  ReadMm3phLine ((unsigned short int *)&v3_mm, IDE1_CS0);
  ReadMm3phLine ((unsigned short int *)&v5_mm, IDE1_CS0);
}
```

Under the present architecture a check-sum is needed in order to verify the accuracy of the transferred data between nodes.

3.9 I/O Card Performance

The inherent time for the write operation of a byte through the I/O interface card is shown in Figure 3-12 on page 40, the data was acquired with a Tektronik 340A digital Scope.

For power simulation in which the links between substations usually involve no more than a double three phase circuit, it is much more convenient to design a communication interface which achieves a scant latency time. This approach is more convenient even though the final data transfer rate may become lower than that of a high speed communication network. This situation is especially relevant to our case since thanks to the decoupling introduced by the transmission links, only a few bytes per time step need to be transferred to the other subsystem node.

If the load distribution among the PC cluster were to involve a high number of transmission links between solver nodes, such as in the case of lower-voltage distribution systems could be feasible the implementation of a high speed communication network. This is not the case, however of High voltage power systems for which the presented topology works appropriately.

While a typical Myrynet communication network can achieve up to 138 Mb/sec with a round trip latency roundtrip of 20 microseconds [7], the I/O interface card presented in this work achieves 4.5 Mb/sec with a round trip latency of around 1.5 microseconds. For example, while the Myrynet network is still under configuration, the developed I/O card interface is already able to transfer all the information needed for the calculation. This round trip IDE latency is fixed by the CPU bus frequency. The faster the bus the smaller the latency introduced.

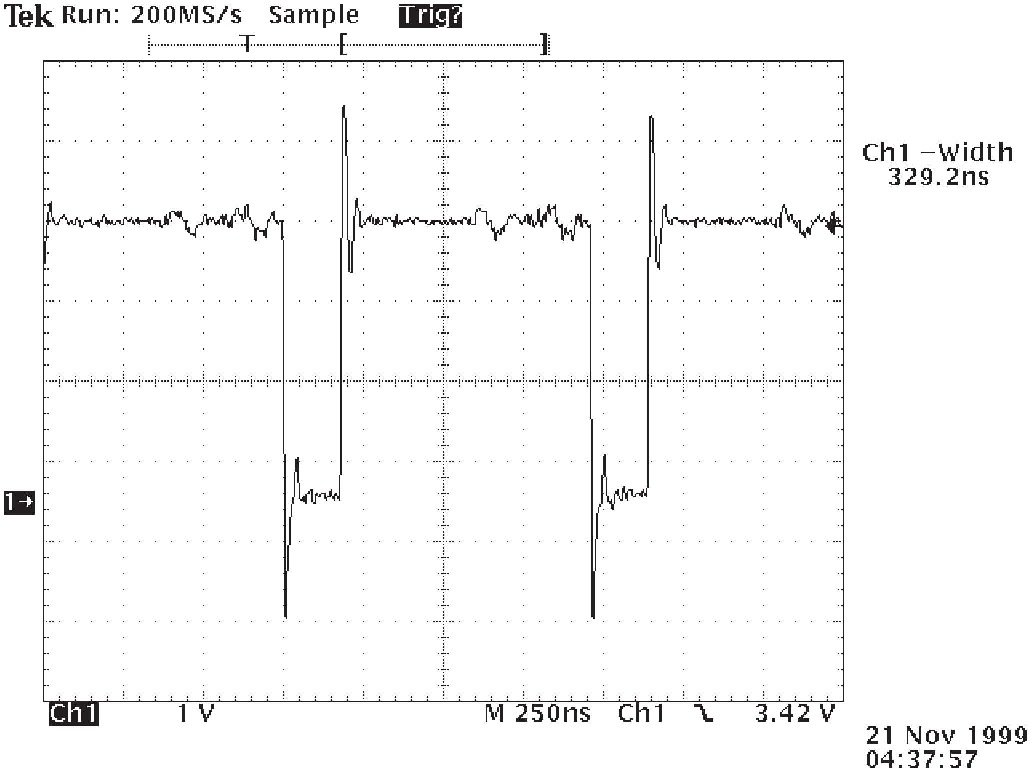


Figure 3-12. *I/O interface Write operation*

Once the links layout is defined in the simulator, the associated communication time is constant, independently of the number of computers added to the array. SeeTable 3-4.

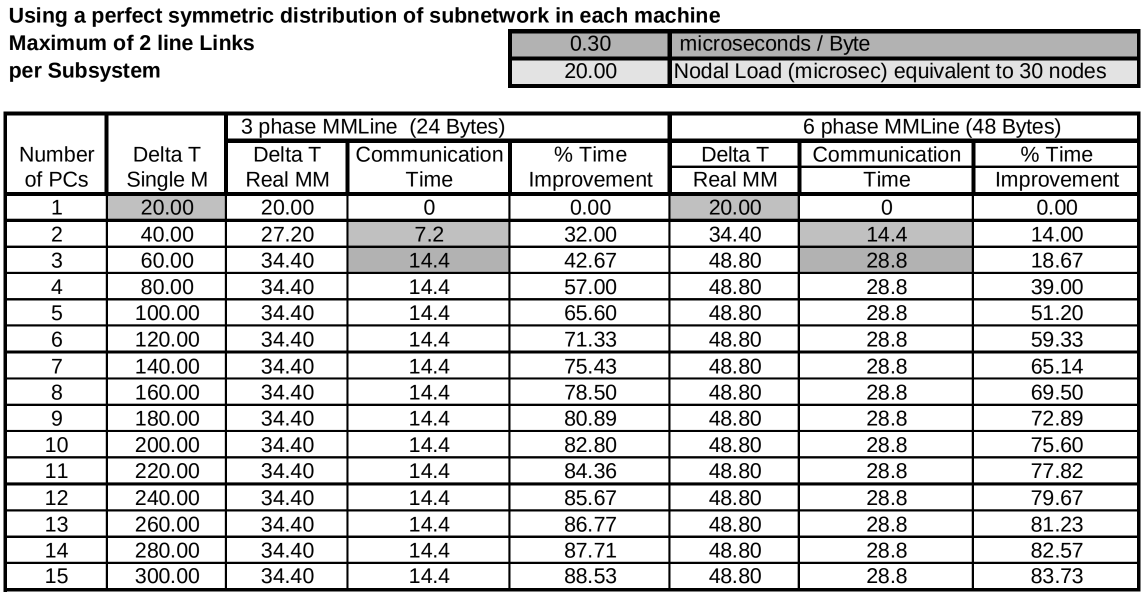
Table 3-4. *Communication times vs. links layout*

Links per subsystem node	3 Phase Line Single circuit	3 Phase Line Double circuit
1	7 µs	14 µs
2	14 µs	28 µs

As it can be observed in Table 3-4 on page 40, in the case of a substation node with one incoming and one outgoing three-phase double-circuit link, the time involved in the communication is 28 microseconds, a few microseconds more than the needed time to configure a Myrynet high speed communication network.

Table 3-5 below, and Table 3-13 on page 42 show the relation between the number of nodes connected, the timings, and the connection layout of the nodes in the array. It is clear that for a given load size —expressed in terms of the computational time needed to solve it— applied to each node element of the PC cluster array, there is a defined time step which can be implemented simulating in real-time, independently of the number of PCs added to the array.

Table 3-5. *Communication Times vs. Number of Subsystem Nodes*[6]



Using a perfect symmetric distribution of subnetwork in each machine
Maximum of 2 line Links
per Subsystem

0.30	microseconds / Byte
20.00	Nodal Load (microsec) equivalent to 30 nodes

Number of PCs	Delta T Single M	3 phase MMLine (24 Bytes)			6 phase MMLine (48 Bytes)		
		Delta T Real MM	Communication Time	% Time Improvement	Delta T Real MM	Communication Time	% Time Improvement
1	20.00	20.00	0	0.00	20.00	0	0.00
2	40.00	27.20	7.2	32.00	34.40	14.4	14.00
3	60.00	34.40	14.4	42.67	48.80	28.8	18.67
4	80.00	34.40	14.4	57.00	48.80	28.8	39.00
5	100.00	34.40	14.4	65.60	48.80	28.8	51.20
6	120.00	34.40	14.4	71.33	48.80	28.8	59.33
7	140.00	34.40	14.4	75.43	48.80	28.8	65.14
8	160.00	34.40	14.4	78.50	48.80	28.8	69.50
9	180.00	34.40	14.4	80.89	48.80	28.8	72.89
10	200.00	34.40	14.4	82.80	48.80	28.8	75.60
11	220.00	34.40	14.4	84.36	48.80	28.8	77.82
12	240.00	34.40	14.4	85.67	48.80	28.8	79.67
13	260.00	34.40	14.4	86.77	48.80	28.8	81.23
14	280.00	34.40	14.4	87.71	48.80	28.8	82.57
15	300.00	34.40	14.4	88.53	48.80	28.8	83.73

[6] Timings for Pentium II 400 Mhz, PIO mode 2.

This feature is advantageous, since it allows the simulation of systems of any size with the desired time step just by defining correctly the basic load block to be assigned to each PC in the cluster and connecting the necessary PC solvers to the array.

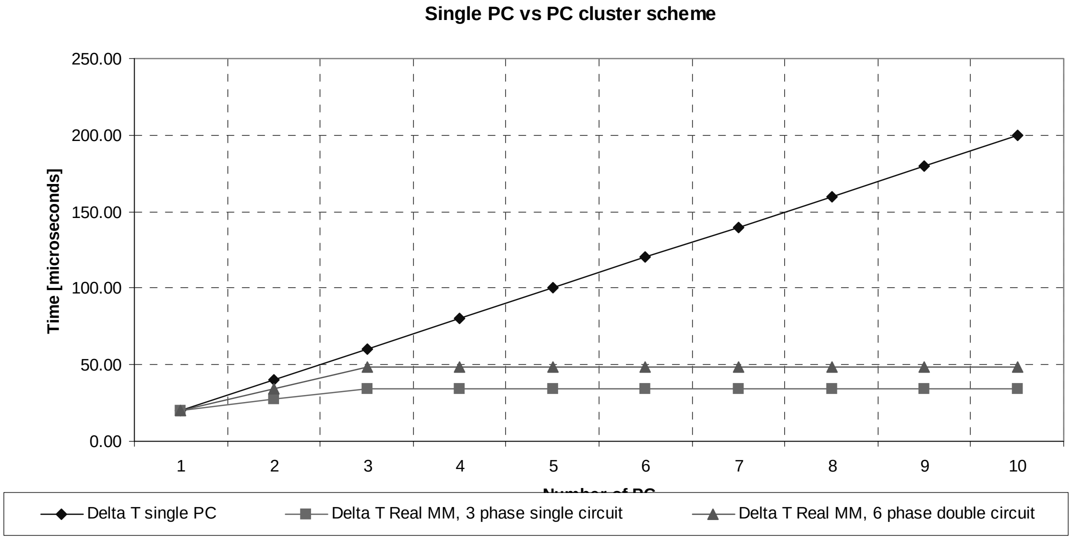


Figure 3-13. *Communication Timings, Single PC vs. PC cluster solution*

4 TEST CASES

Test case 1 and its subcases are described in this chapter. Each test case was run first with a single PC using the RTNS software, applying the minimum possible time step to achieve real-time performance. After this, the same system was pre-processed to run with a PC cluster scheme running the RTDNS software. Two cases were considered. The first case used the same time step as the generic single PC case to verify the accuracy of the distributed scheme implementation. The second case adopted the minimum possible time step to achieve real-time performance with a PC cluster scheme in order to quantify the speed gain of the proposed distributed architecture.

The adopted nomenclature is as follows:

- Test Case 1 - Full System simulated in one PC using RTNS. See Figure 4-1 on page 45.
- Test Case 1a - Subsystem of the full system, simulated in Node I of the PC cluster array. See Figure 4-2 on page 46.
- Test Case 1b - Subsystem of the full system, simulated in Node II of the PC cluster array. See Figure 4-2 on page 46.

Test Case 1 is a 54 node/88 Branch system which includes sources, three phase transmission lines featured in single and double circuits, MOVs, and Thevenin equivalent circuits for certain parts of the network. When a PC cluster solution is implemented, one of the three-phase transmission lines is chosen as the Link Line between subsystem calculation nodes. See Figure 4-2 on page 46. Under these circumstances, the load of the subsystem is not symmetric and it does not produce the most effective distribution. In spite of this situation, the speed gain is still very good. For instance, in Test Case 1 the speed gain under the tested load distribution is 32.89%, while under a perfectly symmetrical distribution of the load the speed gain can reach a value around 34,7%[1].

The obtained speed performances for Test Case 1 are shown in Table 4-1. To perform the simulations, Pentiums II 400 Mhz, Asus P3B motherboards, 64 Mb RAM, Phar Lap TNT ETS 8.5 [11] as the real-time operating system, and RTDNS were used. The present times include 6 outputs for the single-PC case, while for each subsystem case -1a & 1b- 3 outputs were included.

Table 4-1. *Test Case 1 timing results*

Architecture	**Nodes per Machine**	**Minimum Time Step to achieve Real Time**	**Adopted Time Step for test simulations**
Single PC	54	68.7 μsec	70 μsec
PC Cluster	24	43.6 μsec	50 μsec
scheme with two Nodes	30	46.1 μsec	50 μsec
	Speed Gain	**32.89%**	

A single phase fault was applied during 10 milliseconds in Test Case 1. To compare the accuracy of RTDNS against RTNS, the results obtained by both the single PC and PC

[1] Adopting a PC cluster layout with single three phase Line Link and perfect Symmetric subsystem node Load.

cluster architectures using the same time step were plotted on the same graph. See Figure 4-7 on page 49. A detailed zoom graph is shown in Figure 4-8 on page 50. There is no visual difference between both results, as it can be seen in the detailed zoom graph. The difference in percentage between the full system simulated in only one PC using RTNS and the same case distributed in two machines is zero. This proves that the Link Line model is correct, and that the I/O interface card does not introduce any error in the simulation result. RTNS was validated against Microtran EMTP in [4].

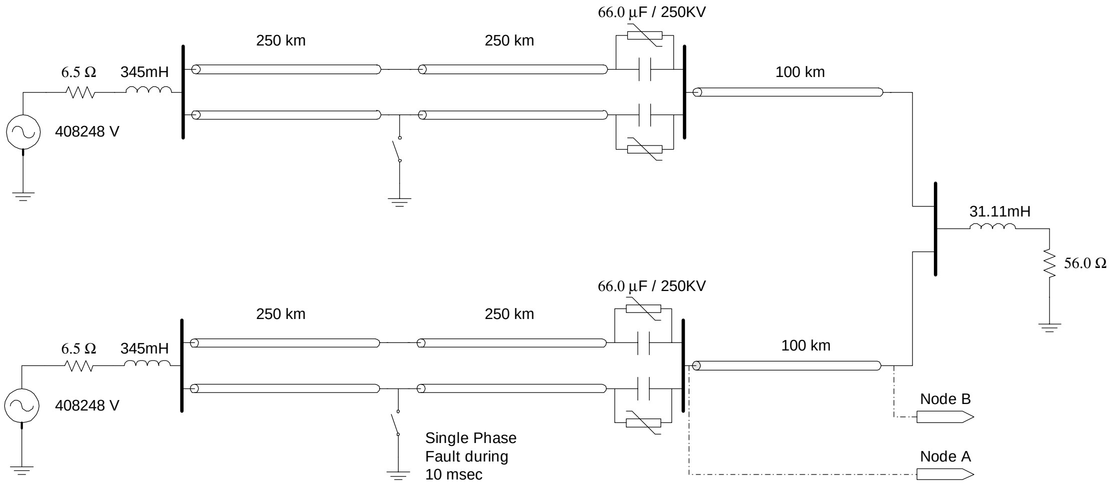


Figure 4-1. *Test Case 1*

A comparison between running the same system at the delta t required by the single-PC solution of RTNS, which is 70 microseconds, and the two-PC-solution of RTDNS, which is a 50 microseconds, is shown in Figure 4-9 on page 51.

Figure 4-6 on page 48, presents the execution times of Test case 1 applying both single PC and PC cluster scheme solutions. The timing difference between the PC cluster nodes is due to the non-symmetric distribution of the load. The minimum possible real-time step is defined for the perfect symmetric load distribution and it is located between the presented node 1 and node 2 timings.

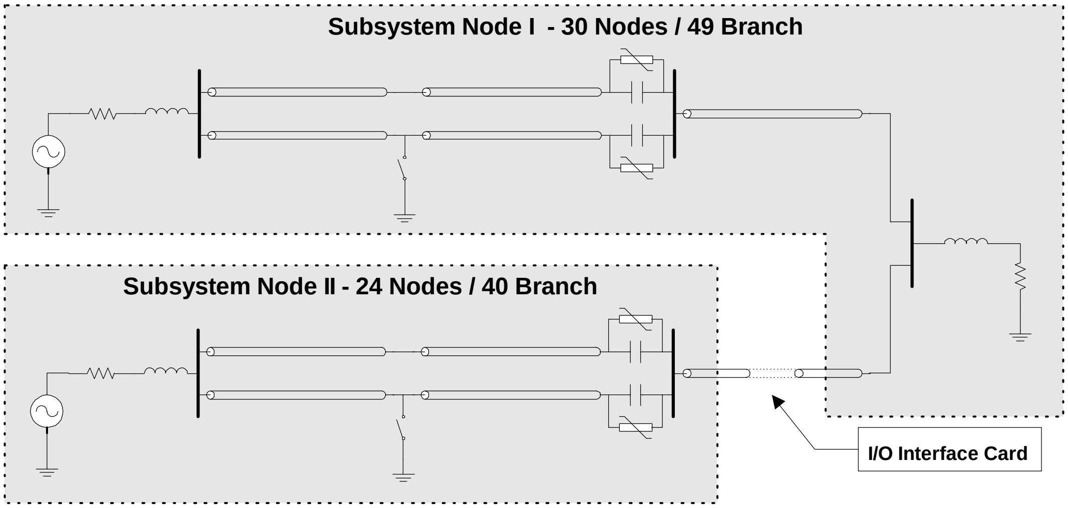

Subsystem Node I - 30 Nodes / 49 Branch
Subsystem Node II - 24 Nodes / 40 Branch
I/O Interface Card

Figure 4-2. *Test Cases 1a & 1b*

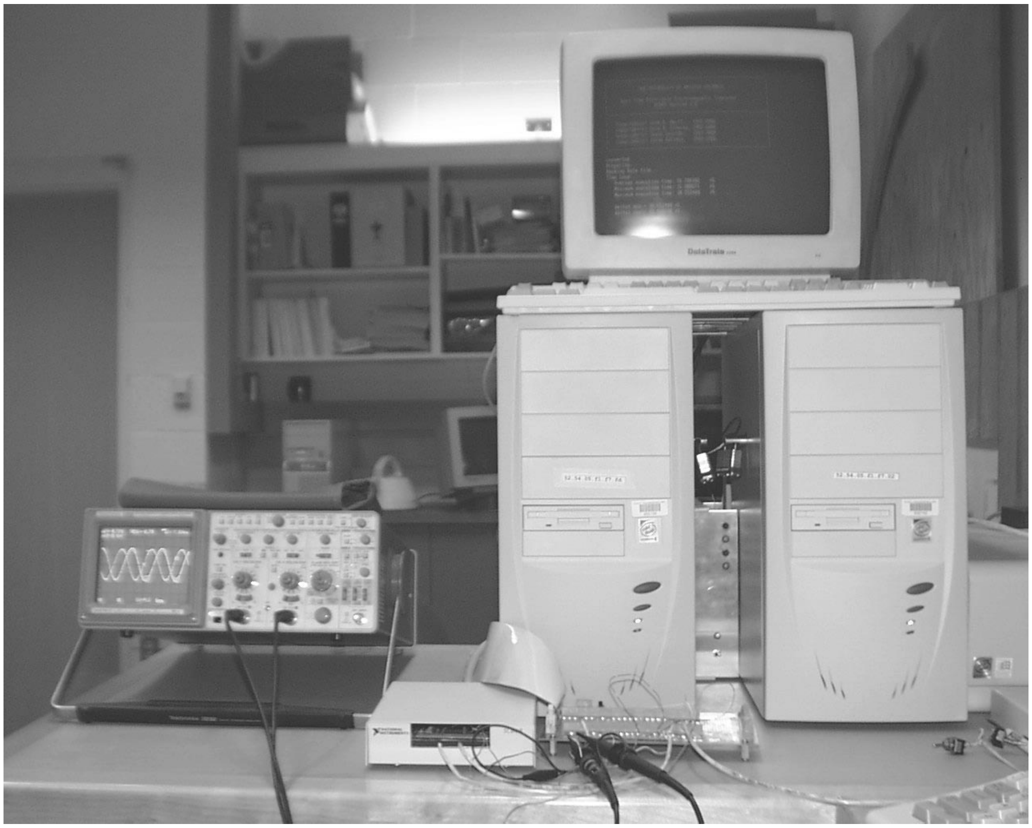


Figure 4-3. *PC Cluster of two computers running Test Case 1a & 1b, front view*

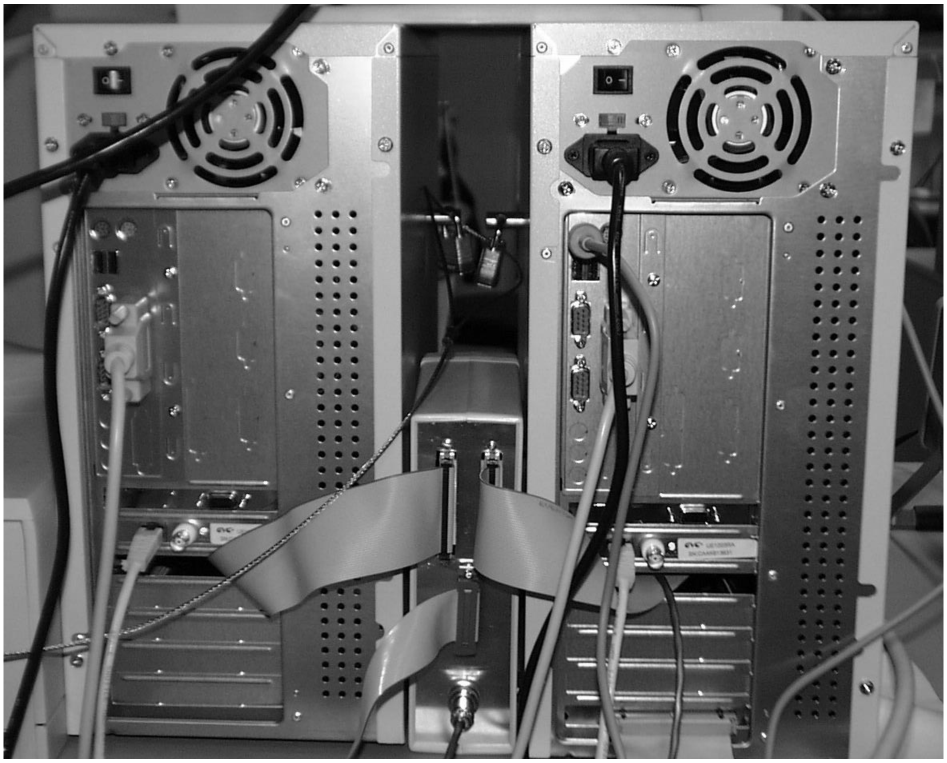


Figure 4-4. *PC Cluster of two computers, rear view*

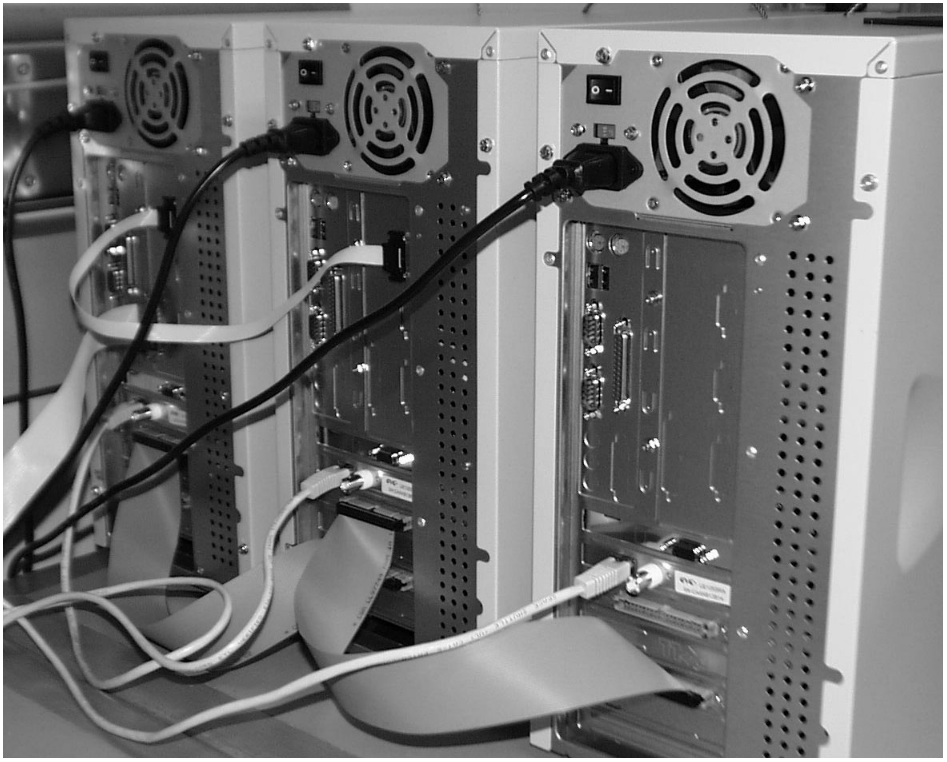


Figure 4-5. *PC Cluster of three computers*

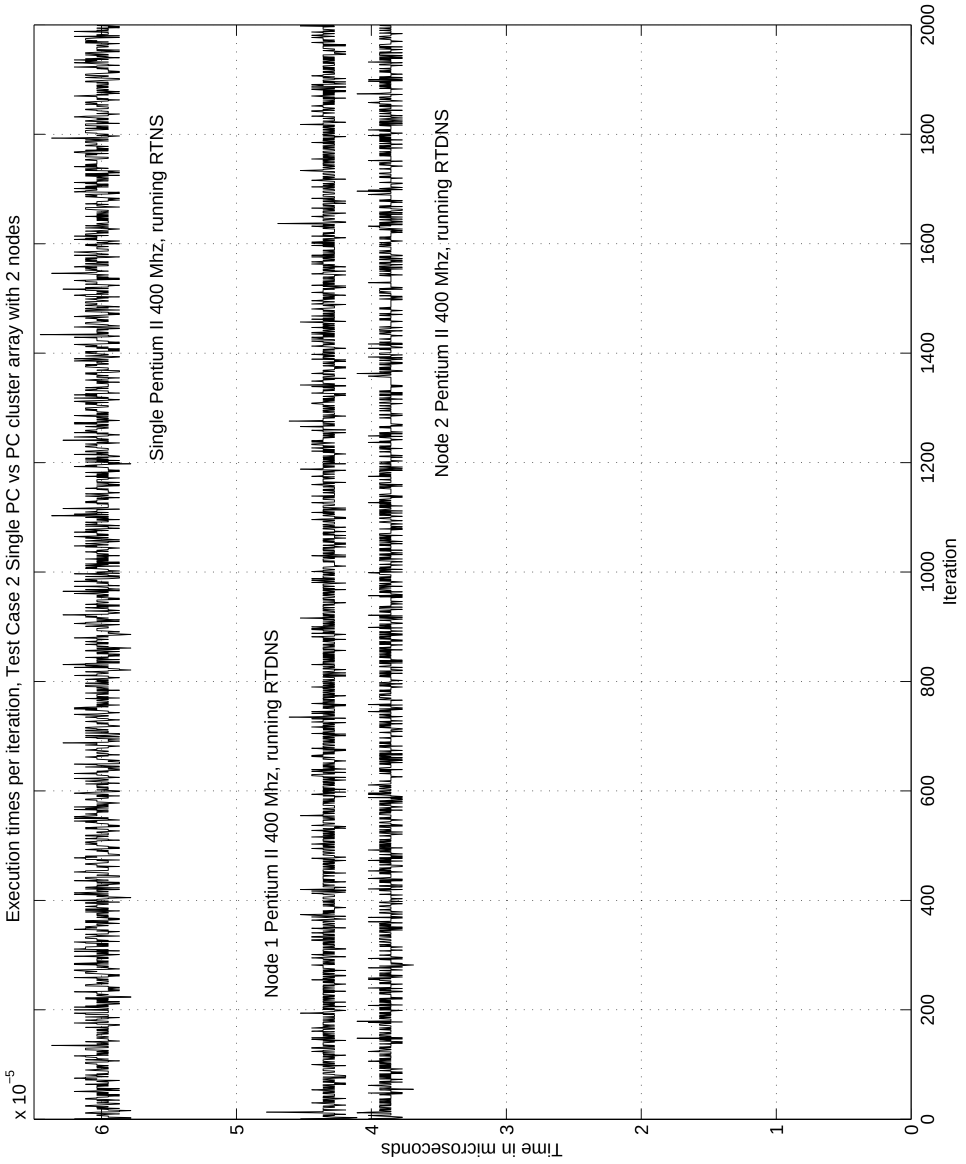


Figure 4-6. *Execution times Single PC vs. PC clustered scheme*

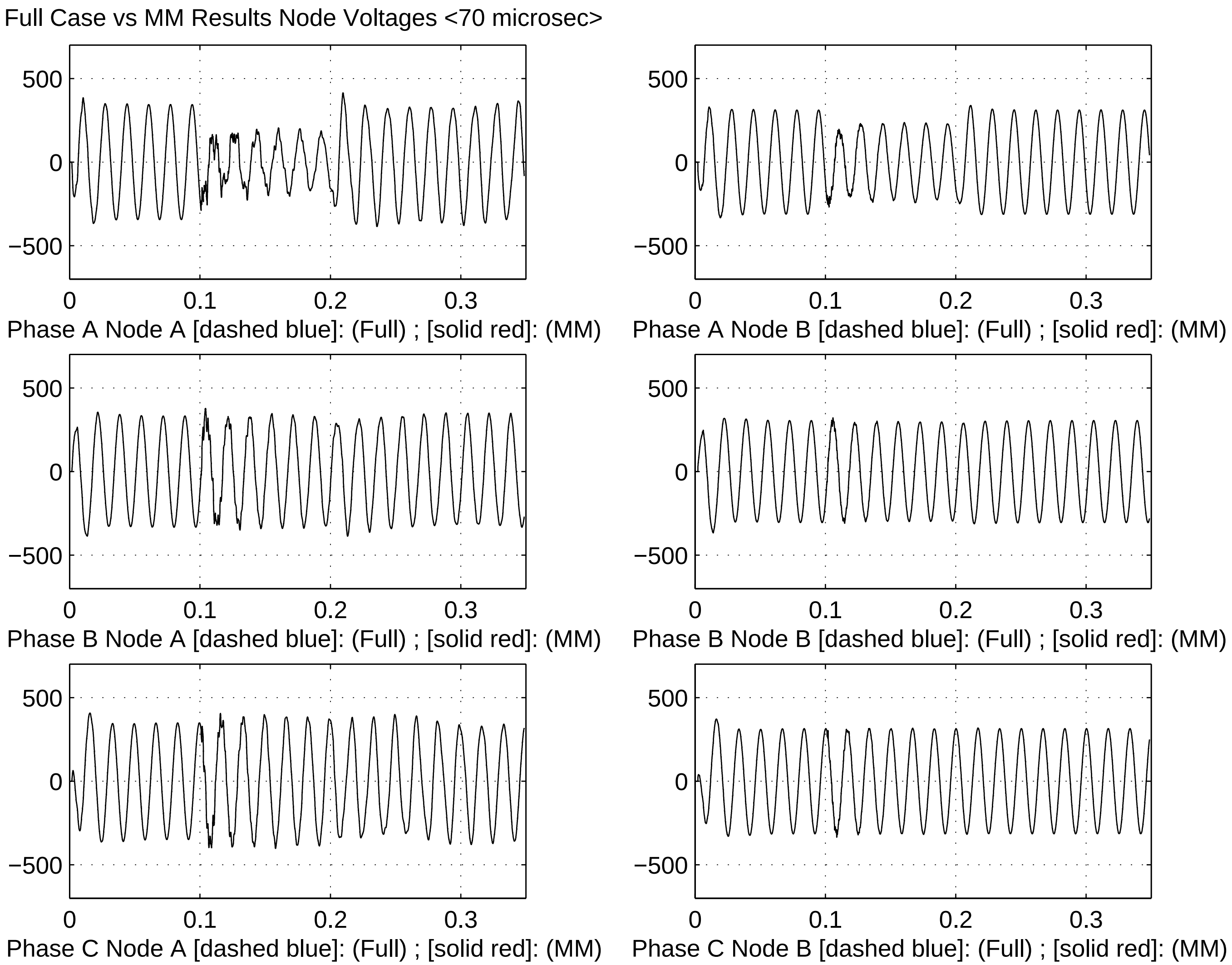


Figure 4-7. *Single PC vs. PC cluster, Solution using the same time step*

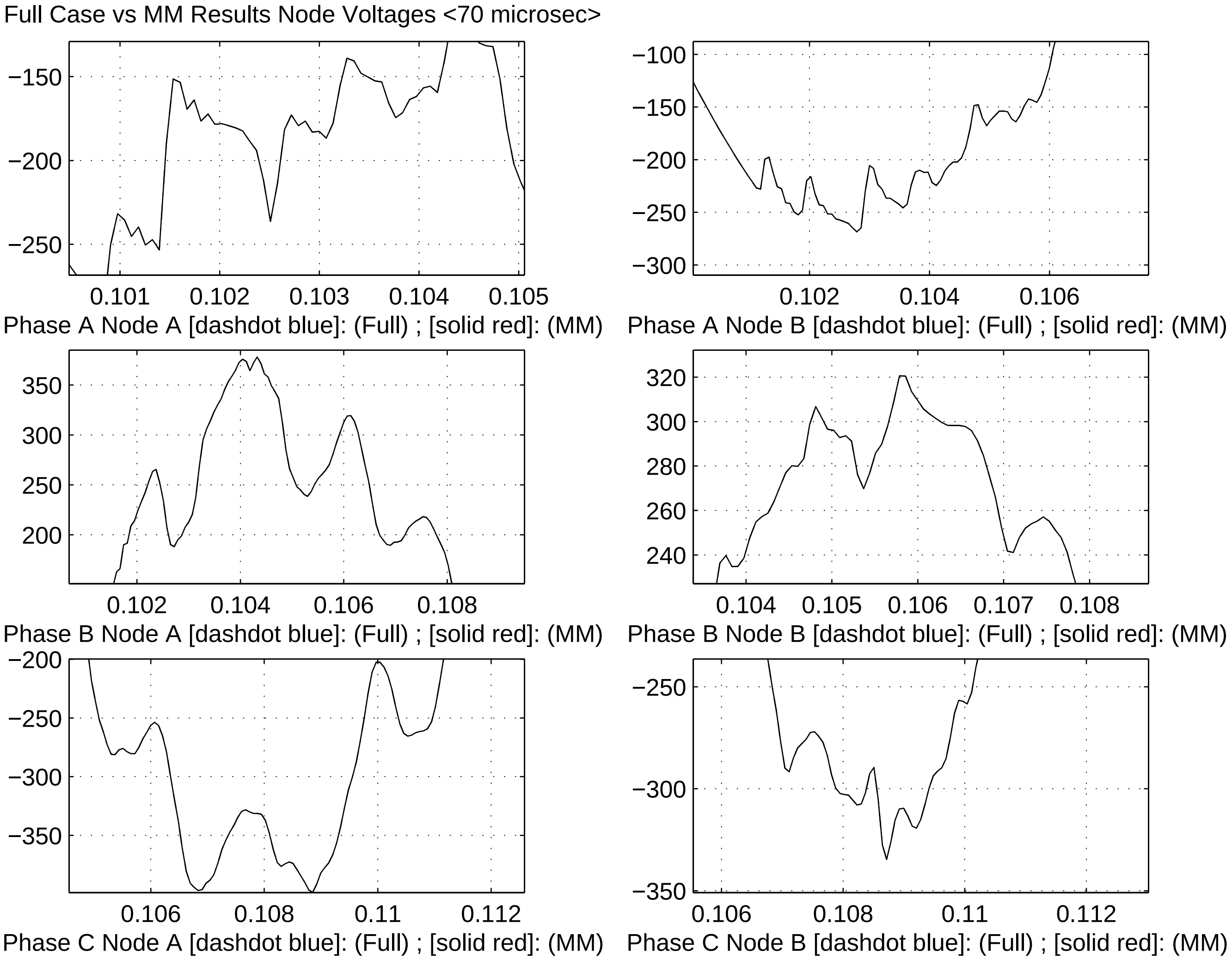


Figure 4-8. *RTNS vs. RTDNS, Plots are superimposed and indistinguishable*

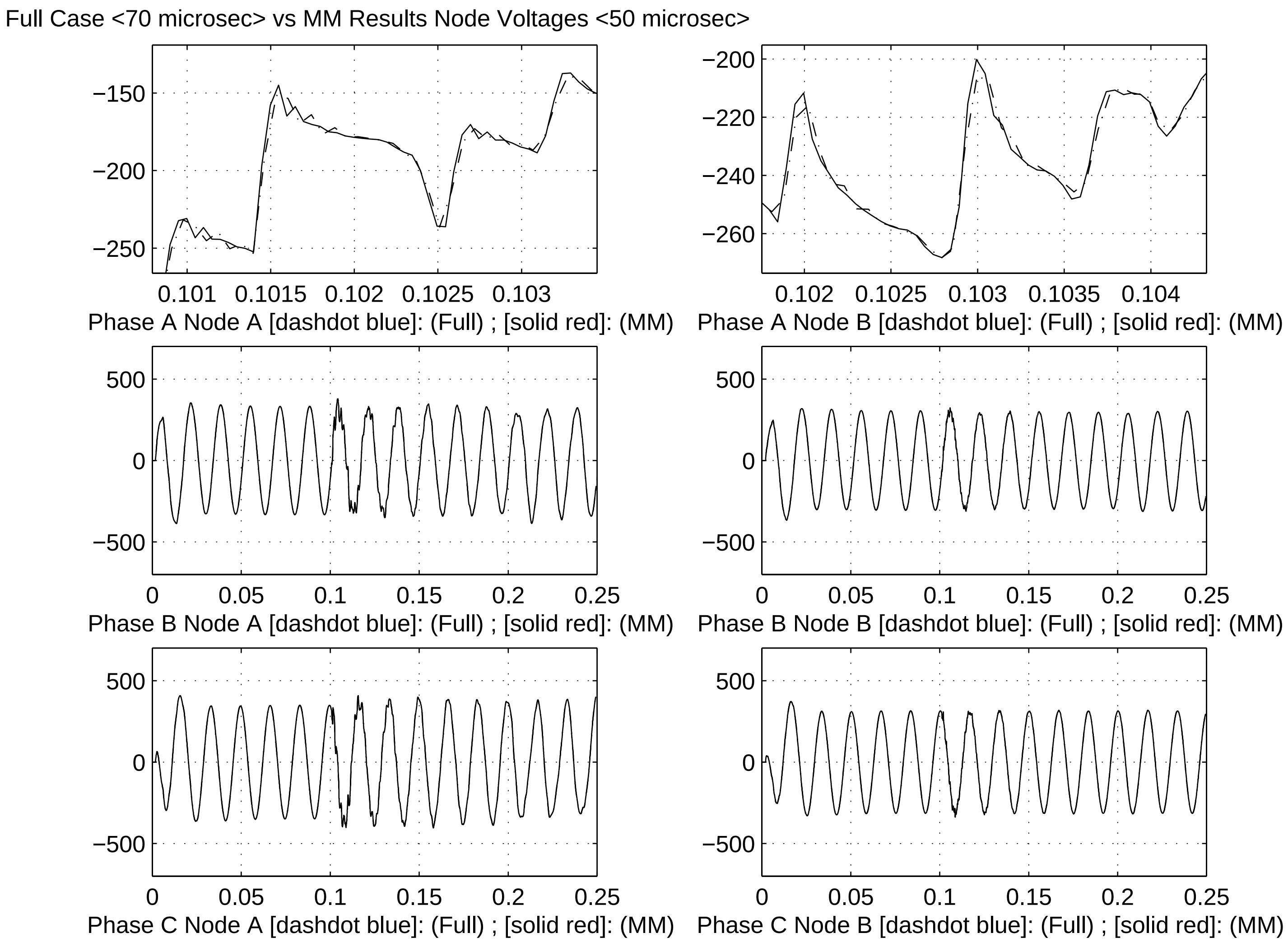


Figure 4-9. *Single PC (70 microsec) vs. PC Cluster (50 microsec)*

The obtained analog output voltages at the evaluated nodes by using a multi I/O board from National Instruments, the AT-MIO-16 are presented in Figure 4-10.

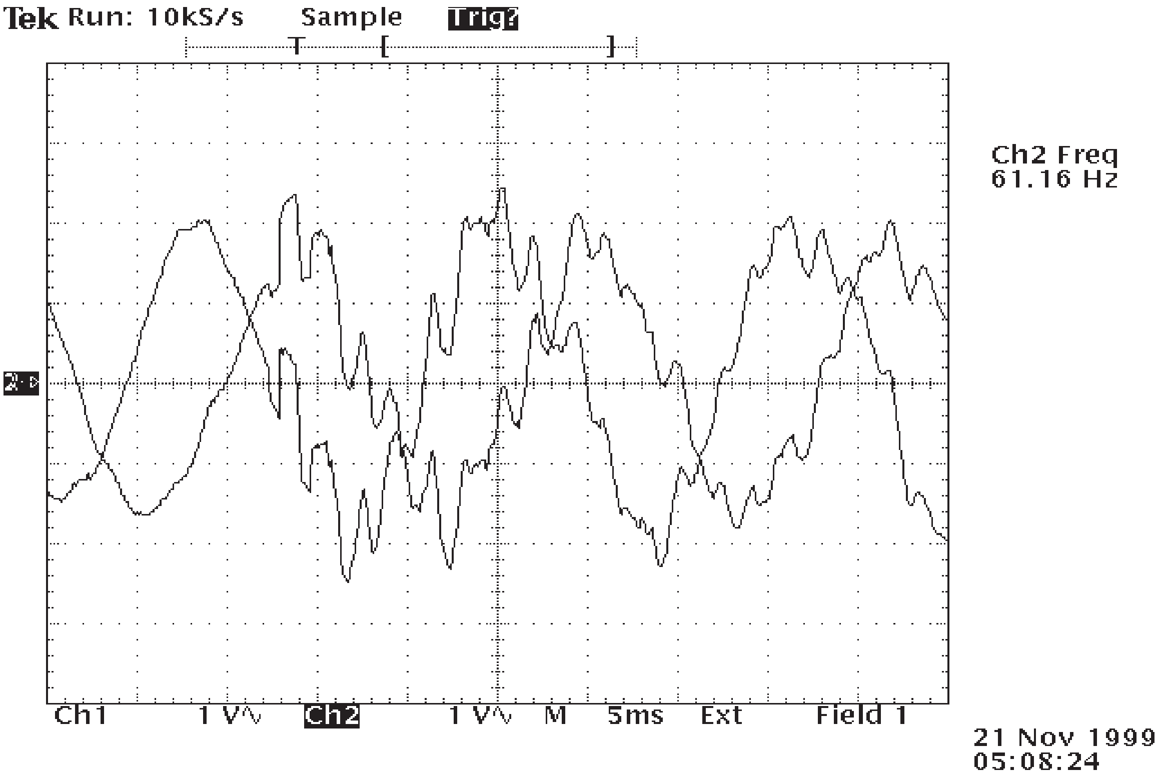


Figure 4-10. *Analog Outputs from test case1, PC cluster simulation*

Also, Test case 2 and its subcases are presented. The simulated systems using a PC cluster of three Pentium II 400 Mhz is shown in Figure 4-11 on page 53. The speed gain is presented in Figure 4-2 on page 53. Since the load distribution is non symmetric, the obtained speed gain differs from the theoretical 42%.

Table 4-2. *Test Case 2 timing results*[a]

Architecture	Nodes per Machine	Minimum Time Step to achieve Real Time	Adopted Time Step for test simulations
Single PC	78	60 µsec	65 µsec
PC Cluster	30	33.42 µsec	40 µsec
with three	18	37.77 µsec	40 µsec
Solver Nodes	30	33.44 µsec	40 µsec
	Speed Gain	**37.05%**	

[a] Simulations without Analog Outputs and using Pentium II 400 Mhz, PIO mode 2 and non symmetric load.

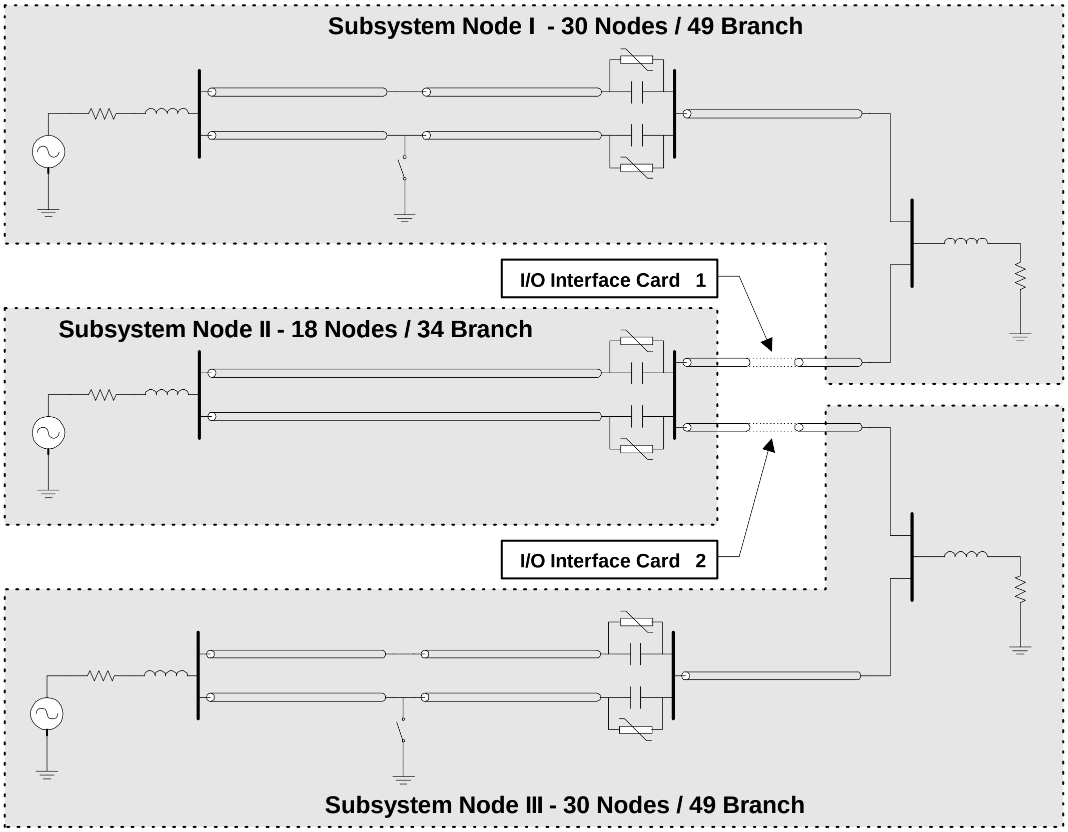

Subsystem Node I - 30 Nodes / 49 Branch
I/O Interface Card 1
Subsystem Node II - 18 Nodes / 34 Branch
I/O Interface Card 2
Subsystem Node III - 30 Nodes / 49 Branch

Figure 4-11. *Test Cases 2a, 2b & 2c*

5 CONCLUSIONS AND RECOMMENDATIONS

The presented thesis attempts to introduce an efficient and accurate PC-cluster solution for real-time network simulations using off-the-shelf equipment plus an efficient I/O interface to perform the communication between the nodes of the array.

The proposed solution layout shows a better and less expensive performance than the only current competing solution in the field in PC cluster arrays. An extra relevant time saving is introduced by a more efficient solver algorithm solution.

The constant inherent time of the communication interface represents a great advantage since an unlimited number of PC's can be connected to the array without affecting the communication time in the time step solution. So far, a PC cluster of up to three PCs has been tested. The present RTDNS software allows communication between nodes of the PC cluster with up to two computers for each subsystem node, achieving real-time performance for three-phase single-circuit links. A simple CPU upgrade to a Pentium III 600 Mhz would allow the simulation of systems with up to two double-circuit links.

The importance of the multi-PC's synchronization should be stressed, since even if small differences, like one time step, were allowed, they could introduce numerical oscillations and accumulated run-off errors. To address this problem a robust external and shared synchronism source is implemented based on a programmable internal interval timer CHMOS —82C54—.

Part of the appeal of the proposed solution is that the concept can perfectly be applied to future faster CPU busses with minor or no modifications.

Future research should be done to develop:

- A better and friendlier user interface for the simulator.
- An implementation of new models for full frequency dependent transmission lines in real time and their corresponding Link Line version.
- An implementation of data compression algorithms to increase the capabilities of the I/O interface.
- An exploration of Direct Memory Access[1] performances.

A crucial topic that calls for future research is related to the development of a *Load Distribution* algorithm which automatically finds the optimal load distribution among the subsystem nodes.

In order to implement bigger PC cluster arrays, it is necessary to perform the distribution of the data cases among the PC cluster array using a more flexible scheme, such as FTP or TCP/IP.

[1] A method for transferring data between an external device and memory without interrupting program flow or requiring CPU intervention

References

[1] H.W. Dommel, (April 1969).Digital computer solution of electromagnetic transients in single and multiphase networks, IEEE Trans. on Power Apparatus and Systems, Vol. PAS-88, No. 4, pp 388-399.

[2] H.W. Dommel, (1992). EMTP Theory Book, (2nd ed.), Vancouver, Microtran Power System Analysis Corporation.

[3] J.R. Marti, L.R. Linares, (August 1994). Real Time EMTP-based transients simulation. IEEE Trans. on Power Systems, Vol. 9, N0.3, pp. 1309-1317.

[4] L.R. Linares R., (April 1993). A Real Time Simulator for Power Electric Networks, M.A.Sc. Thesis, UBC Library.

[5] W.H. Press, S.A. Teukolsky, W.T. Vetterling, B.P. Flannery, (1997). Numerical Recipies in C. (2nd. ed.), Cambridge.

[6] K.K. Fung, S.Y.R. Hui, (1996). Transputer simulation of decoupled electrical circuits. Mathematics and Computers in simulation 42, 1-13.

[7] Hiroshi Tezuca, Francis O' Carroll, Atsushi Hori and Yutaka Ishikawa, (1997). Pin-down Cache : A virtual Memory Management Technique for zero-copy Communication.

[8] Yasushi Fujimoto, Yuan Bin, Hisao Taoka, (1999). Real-time Power System Simulator on a PC cluster, IPST'99 Budapest.

[9] J. Calviño-Fraga, (June 1999). Implementation of a Real Time Simulator for Protective Relay Testing, M.A.Sc. Thesis, UBC Library.

[10] Fromonto, Levacher, Strunz, (1999). An efficient Parallel Computer Architecture for real time simulations of electromagnetic transients in power systems Electricité de France, 31st North American Power Symposium, 490 - 496.

[11] Phar Lap, (1999). Phar Lap TNT Embedded ToolSuite,
Available: http://www.pharlap.com/

[12] IDT, (1999). IDT 7132/42 Data Sheet,
Available: http://www.idt.com/products/pages/Multi-Port-7132.html

[13] National Instrument, (1999). CVI home page
Available: http://www.ni.com/cvi/

[14] Martí, J. R., (1991). Simplified Updating Schemes for EMTP's models, The University of British Columbia. Department of Electrical Engineering Internal Report.

[15] Intel, (1999). IDE Controller Functional Description.
Available:http://developer.intel.com/design/intarch/techinfo/440bx/ide-func.htm#716485

[16] Martí, J. R., Linares, L.R., Calviño-Fraga, J., Dommel, H. W., (1998). OVNI: an Object Approach to Real-Time Power System Simulators, Proceedings of the 1998 International Conference on Power System Technology, Powercon'98 Beijing, China, April 18-21, pp. 977-981.

[17] National Instruments, (September 1994). AT-AO-6/10 User Manual.

[18] Shanley, T., & Anderson, D.(1997). PCI System Architecture (3rd ed.), Addison-Wesley.

[19] Texas Instrument, (1985). The TTL Data Book (vol. 2).

[20] D’Ajuz, A., Fonseca, C., Carvalho, F.M., Filho, J., Dias, L.E., Pereira, M., et al., (1987). Transitorios Electricos e Coordenação de Isolamento, aplicação em sistemas de potência de alta tensão, Universidade Federal Fluminense, Editora Universitária.

Appendix I. Schematics and PCB Files

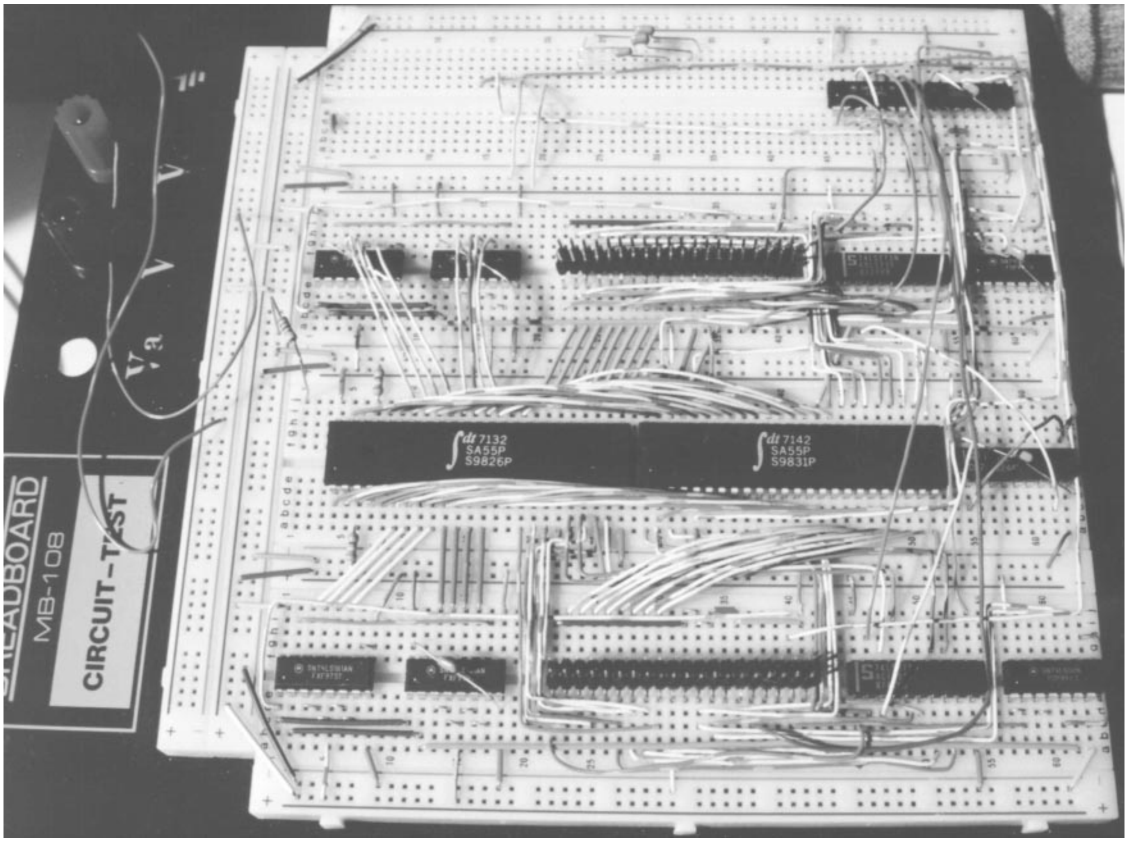


Figure I-1. *Top PCB Plot, I/O Interface Card*

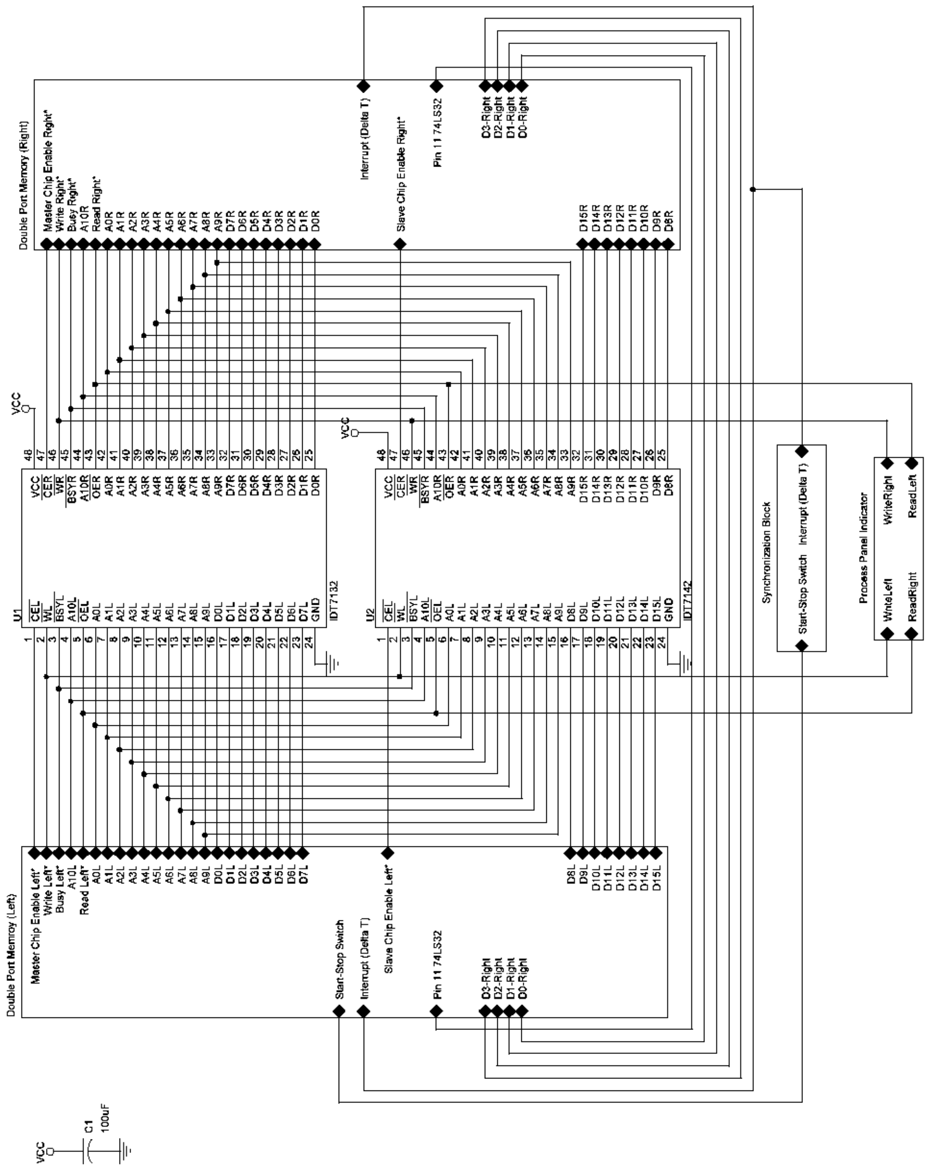


Figure I-2. *General Block Schematic of the IDE Interface Card*

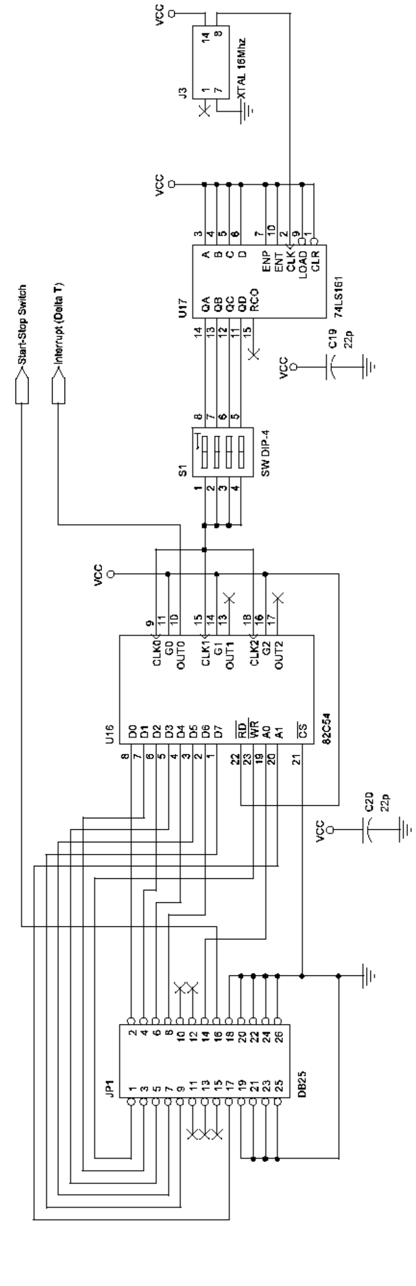


Figure I-3. *Schematic of the Synchronization Block*

Final Netlist I/O Interface Card

```
Revised: June 21, 1999
E:\JORGE\ORCAD PROJECTS\IDE_INTERFACE_FULL_SCHRevision:
[C1      cap100   22p]
[C10     cap100   22p]
[C11     cap100   22p]
[C12     cap100   22p]
[C2      cap100   22p]
[C3      cap100   22p]
[C4      cap100   22p]
[C5      cap100   22p]
[C6      cap100   22p]
[C7      cap100   22p]
[C8      cap100   22p]
[C9      cap100   22p]
[J1      molex40  CON40A]
[J2      molex40  CON40A]
[J3      Dip14    XTAL 16 Mhz]
[JP1     Pattern  HEADER 13X2]
[R1      res300   390]
[R2      res300   390]
[S1      dip8     SW DIP-4]
[U1      dip16    74LS161]
[U10     dip48    IDT7142]
[U11     dip20    74LS244]
[U12     dip14    74LS32]
[U13     dip14    74LS00]
[U14     dip24    82C54]
[U15     dip16    74LS161]
[U2      dip16    74LS161]
[U3      dip14    74LS00]
[U4      dip14    74LS00]
[U5      dip16    74LS161]
[U6      dip16    74LS161]
[U7      dip48    IDT7132]
[U8      dip20    74LS273]
[U9      dip20    74LS273]
(
N131239
U2,14
U7,42
U10,42
)
(
N131835
S1,2
S1,3
S1,4
U14,9
S1,1
U14,15
U14,18
)
(
N131302
U7,17
J1,15
U8,4
U11,16
)
(
N131389
U10,20
J1,12
)
(
N131929
JP1,8
U14,2
)
(
N131453
U12,1
U7,2
U10,2
J1,23
U3,10
)
(
N131233
U7,7
U1,13
U10,7
)
(
N131236
U6,12
U7,36
U10,36
)
(
N131380
U10,23
J1,18
)
(
N131238
U2,1
U6,1
J2,38
U12,10
U12,12
)
(
N131530
U9,2
U10,34
U7,34
)
(
N131246
U7,11
U5,13
U10,11
)
(
N131868
U15,2
J3,4
)
(
N131499
U7,30
U9,14
J2,7
)
```

```
(
N131258
U6,11
U7,35
U10,35
)
(
N131267
U6,14
U7,38
U10,38
)
(
N131307
U7,19
J1,11
U8,8
U11,12
)
(
GND
C2,2
C1,2
U12,7
U3,7
U4,7
C10,2
C11,2
C12,2
U13,7
U14,12
U15,8
U10,24
U7,24
)
(
N131248
U7,37
U6,13
U10,37
)
(
N131240
U5,12
U7,12
U10,12
)
(
N131251
U7,6
U1,14
U10,6
)
(
N131508
U9,18
U7,32
J2,3
)
(
N131309
U7,21
U8,14
J1,7
)
```

```
(
N131232
U5,11
U7,13
U10,13
)
(
N131623
U10,44
U7,44
U4,11
)
(
N131349
J1,38
U1,1
U5,1
U12,2
U12,4
)
(
N131490
U9,5
U7,33
U10,33
)
(
N131398
J1,6
U10,17
)
(
N131319
U8,18
U7,23
J1,3
)
(
N131386
J1,14
U10,21
)
(
N131311
R1,2
J1,27
U10,3
U7,3
)
(
N131298
U6,2
U2,2
U4,8
)
(
N131813
U13,5
U13,3
)
(
N131529
J2,37
U4,1
U4,2
```

```
U7,47
U10,47
)
(
N131814
U13,6
J1,31
)
(
N131392
J1,10
U10,19
)
(
N131401
U10,16
J1,4
)
(
N131243
U7,9
U1,11
U10,9
)
(
N131266
U7,10
U5,14
U10,10
)
(
N131231
U2,15
U6,10
)
(
N131614
U4,9
U4,3
)
(
N131237
U7,15
U8,5
U10,15
)
(
N131625
J2,8
U10,27
)
(
N131615
U4,6
U4,10
)
(
N131446
U11,3
U7,28
J2,11
U9,8
)
(
N131442
```

```
U11,7
U7,26
J2,15
U9,4
)
(
N131560
U10,32
J2,18
)
(
N131569
U10,29
J2,12
)
(
N131572
J2,10
U10,28
)
(
N131943
JP1,17
U14,20
)
(
N131234
U2,12
U7,40
U10,40
)
(
N131932
U14,1
JP1,9
)
(
N131256
U7,4
U8,6
U10,4
)
(
N131563
U10,31
J2,16
)
(
N131724
U3,4
U3,3
)
(
N131937
JP1,14
U14,19
)
(
N131805
U13,4
U8,19
)
(
N131493
U7,29
```

```
U9,13
J2,9
)
(
N131848
U14,11
U14,14
U14,16
U14,22
)
(
N131686
U8,1
J1,1
)
(
N131818
U13,13
U13,8
)
(
N131300
R2,2
U10,45
J2,27
U7,45
)
(
N131383
U10,22
J1,16
)
(
N131916
JP1,5
U14,5
)
(
N131450
U12,11
U11,19
)
(
N131950
JP1,4
U14,6
)
(
N131799
U12,6
U11,1
)
(
N131245
U2,11
U7,39
U10,39
)
(
N131715
U7,1
J1,37
U3,1
U3,2
U10,1
```

```
)
(
N131345
U8,2
U10,14
U7,14
)
(
N131921
JP1,6
U14,4
)
(
N131441
U11,5
U7,27
J2,13
U9,7
)
(
N131303
U7,20
U8,13
J1,9
)
(
N131924
JP1,7
U14,3
)
(
N131479
U3,8
U3,5
)
(
N131860
U15,11
S1,5
)
(
N131455
U1,2
U3,6
U5,2
)
(
N131680
U4,12
U4,13
U9,6
)
(
N131494
U9,17
U7,31
J2,5
)
(
N131862
U15,13
S1,7
)
(
N131819
```

```
U13,11
J2,31
)
(
N131863
U15,14
S1,8
)
(
N131905
JP1,1
U14,23
)
(
N131395
U10,18
J1,8
)
(
N131807
U9,19
U13,12
)
(
N131454
U7,5
U12,5
J1,25
U10,5
U3,9
)
(
N131575
J2,6
U10,26
)
(
N131358
U8,11
U12,3
)
(
N131444
U11,9
J2,17
U7,25
U9,3
)
(
N131578
U10,25
J2,4
)
(
N131540
U12,8
U9,11
)
(
N131910
U14,8
JP1,2
)
(
N131598
```

```
U12,13
J2,25
U4,4
U7,43
U10,43
)
(
N131350
J1,17
U7,16
U11,18
U8,3
)
(
N131269
U2,13
U7,41
U10,41
)
(
N131597
U12,9
J2,23
U4,5
U10,46
U7,46
)
(
N131911
JP1,3
U14,7
)
(
N131820
J2,1
U9,1
)
(
N131314
U7,18
J1,13
U8,7
U11,14
)
(
N131249
U1,12
U7,8
U10,8
)
(
N131304
U8,17
U7,22
J1,5
)
(
N131566
J2,14
U10,30
)
(
GND POWER
J1,2
J2,19
```

```
J2,26
J2,24
J2,2
J2,22
J2,30
J2,40
JP1,18
U6,8
J1,19
C6,2
JP1,26
U14,21
JP1,20
JP1,22
JP1,24
U5,8
C4,2
U8,10
C7,2
JP1,25
JP1,23
J3,3
JP1,21
JP1,19
J1,24
J1,30
J1,40
J1,26
C5,2
U2,8
J1,22
U11,10
C8,2
C3,2
U1,8
C9,2
U9,10
)
(
VCC
U13,14
U12,14
U15,16
U4,14
R1,1
U3,14
U14,24
U8,20
C7,1
U5,16
C4,1
C12,1
C10,1
C11,1
J3,2
C8,1
U11,20
U6,16
C6,1
U2,16
C5,1
U1,16
C3,1
U13,9
U5,5
```

```
U5,6
U5,9
U5,7
U5,4
U5,3
U1,9
U1,10
U1,4
U1,3
U1,5
U1,6
U1,7
U2,7
U2,4
U2,5
U2,6
U2,3
U2,10
U6,3
U6,4
U2,9
U6,5
U6,7
U6,9
U6,6
U13,1
U9,20
C9,1
U15,10
U15,4
U15,5
U15,6
U15,7
U15,3
U15,1
U15,9
U10,48
C2,1
C1,1
U7,48
R2,1
)
(
ONOFF
U11,11
U11,2
JP1,16
)
(
INTERR
U13,10
U13,2
U14,10
)
(
N131861
U15,12
S1,6
)
(
N131241
U1,15
U5,10
)
```

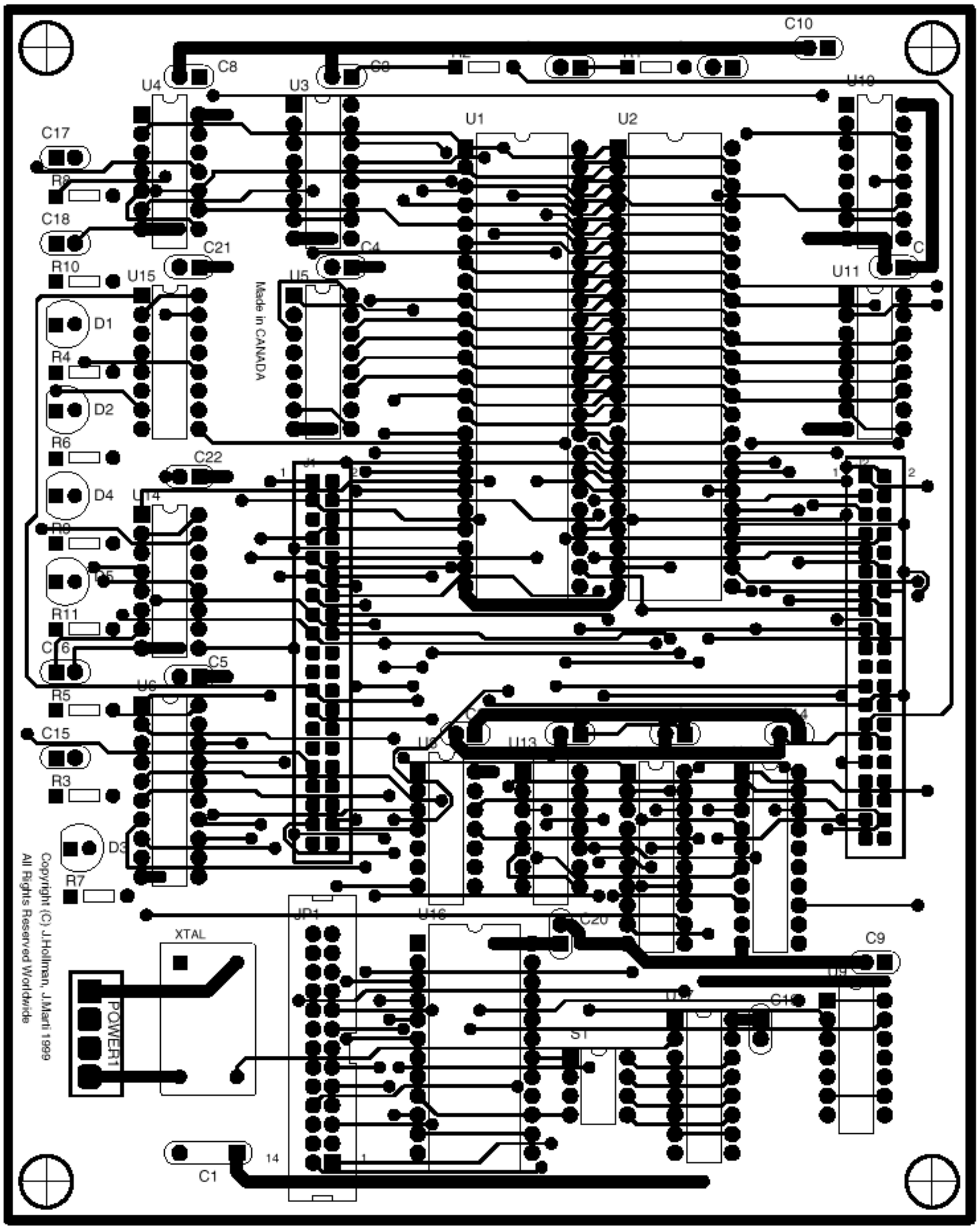


Figure I-4. *Top PCB Plot, I/O Interface Card*

Appendix II. Test Case Files

Preprocessor Input Files

Test Case 1

```
.BEGIN FILE
   .BEGIN GENERAL-DATA
      deltaT: 70.0E-6
      totalTime: 30000
      numLumped: 30
      numLines: 6
      numSources: 6
      numOutNodes: 6
   .END GENERAL-DATA
   .BEGIN LUMPED
      R 6.5 n3a n2a calcCurr: no  MOV: no
      R 6.5 n3b n2b calcCurr: no  MOV: no
      R 6.5 n3c n2c calcCurr: no  MOV: no
      L 345 n2a n1a calcCurr: no  MOV: no
      L 345 n2b n1b calcCurr: no  MOV: no
      L 345 n2c n1c calcCurr: no  MOV: no
      C 66.0 n6a n8a calcCurr: no  MOV: yes 250000
      C 66.0 n6b n8b calcCurr: no  MOV: yes 250000
      C 66.0 n6c n8c calcCurr: no  MOV: yes 250000
      C 66.0 n7a n8a calcCurr: no  MOV: yes 250000
      C 66.0 n7b n8b calcCurr: no  MOV: yes 250000
      C 66.0 n7c n8c calcCurr: no  MOV: yes 250000
      L 31.11 NodBa n12a calcCurr: no  MOV: no
      L 31.11 NodBb n12b calcCurr: no  MOV: no
      L 31.11 NodBc n12c calcCurr: no  MOV: no
      R 56.0 n12a GROUND calcCurr: no  MOV: no
      R 56.0 n12b GROUND calcCurr: no  MOV: no
      R 56.0 n12c GROUND calcCurr: no  MOV: no
      R 6.5 n15a n14a calcCurr: no  MOV: no
      R 6.5 n15b n14b calcCurr: no  MOV: no
      R 6.5 n15c n14c calcCurr: no  MOV: no
      L 345 n14a n9a calcCurr: no  MOV: no
      L 345 n14b n9b calcCurr: no  MOV: no
      L 345 n14c n9c calcCurr: no  MOV: no
      C 66.0 n18a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n18b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n18c NodAc calcCurr: no  MOV: yes 250000
      C 66.0 n19a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n19b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n19c NodAc calcCurr: no  MOV: yes 250000
   .END LUMPED
   .BEGIN LINES
      .BEGIN LINE-0
         phases: 6
         MmLink: 0MmLink: 1
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n1a no n4a no n1b no n4b no n1c no n4c no
                n1a no n5a no n1b no n5b no n1c no n5c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-0
      .BEGIN LINE-1
         phases: 6
         MmLink: 0MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n4a no n6a no n4b no n6b no n4c no n6c no
                n5a no n7a no n5b no n7b no n5c no n7c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-1
      .BEGIN LINE-2
      phases: 3
      MmLink: 0
      Zc: 621.9 275.3 290.9
      delay: 0.4710e-3  0.3416e-3  0.3399e-3
      nodes: n8a no NodBa no n8b no NodBb no n8c no NodBc no
      q-matrix:
         0.58702696 -0.40302458  0.70710678
         0.55427582  0.82086139  0.00000000
         0.58702696 -0.40302458 -0.70710678
   .END LINE-2
   .BEGIN LINE-3
      phases: 6
      MmLink: 0
      Zc: 987.9 328.4 275.9 222.6 237.2 244.1
      delay: 1.4069e-3    0.8699e-3   0.8506e-3
             0.8418e-3    0.8418e-3   0.8420e-3
      nodes: n9a no n16a no n9b no n16b no n9c no n16c no
             n9a no n17a no n9b no n17b no n9c no n17c no
      q-matrix:
         0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
         0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
         0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
         0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
         0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
         0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
   .END LINE-3
   .BEGIN LINE-4
      phases: 6
      MmLink: 0
      Zc: 987.9 328.4 275.9 222.6 237.2 244.1
      delay: 1.4069e-3    0.8699e-3   0.8506e-3
             0.8418e-3    0.8418e-3   0.8420e-3
      nodes: n16a no n18a no n16b no n18b no n16c no n18c no
             n17a no n19a no n17b no n19b no n17c no n19c no
      q-matrix:
         0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
         0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
         0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
         0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
         0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
         0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
   .END LINE-4
   .BEGIN LINE-5
      phases: 3
      MmLink: 0
      Zc: 621.9 275.3 290.9
      delay: 0.4710e-3  0.3416e-3  0.3399e-3
      nodes: NodAa no NodBa no NodAb no NodBb no NodAc no NodBc no
      q-matrix:
         0.58702696 -0.40302458  0.70710678
         0.55427582  0.82086139  0.00000000
         0.58702696 -0.40302458 -0.70710678
   .END LINE-5
.END LINES
.BEGIN SOURCES
   408248   0 n3a
   408248  120 n3b
   408248 -120 n3c
   408248   0 n15a
   408248  120 n15b
   408248 -120 n15c
.END SOURCES
.BEGIN SWITCHES
   total: 6
   n5a GROUND close: 1 open: 1
      close: 3000
      open: 3600

   n5b GROUND close: 1 open: 1
      close: 3000
      open: 3600

   n5c GROUND close: 1 open: 1
      close: 3000
      open: 3600

   GROUND n17a close: 1 open: 1
      close: 0.10
      open: 0.20

   GROUND n17b close: 1 open: 1
```

```
         close: 3000
         open: 3600

      GROUND n17c close: 1 open: 1
         close: 3000
         open: 3600
   .END SWITCHES
   .BEGIN OUTPUT
      NodAa NodAb NodAc
      NodBa NodBb NodBc
   .END OUTPUT
   .BEGIN DACS
      total: 6
      .BEGIN T0
         type: CCVT
         port: 0
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t0
      .BEGIN T1
         type: CCVT
         port: 1
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t1
      .BEGIN T2
         type: CCVT
         port: 2
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t2
      .BEGIN T3
         type: CCVT
         port: 3
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t3
      .BEGIN T4
         type: CCVT
         port: 4
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t4
      .BEGIN T5
         type: CCVT
         port: 5
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t5
   .END DACS
.END FILE
```

Test Case 1a

```
.BEGIN FILE
   .BEGIN GENERAL-DATA
      deltaT: 50.0E-6
      totalTime: 30000
      numLumped: 18
      numLines: 4
      numSources: 3
      numOutNodes: 3
   .END GENERAL-DATA
   .BEGIN LUMPED
      R 6.5 n3a n2a calcCurr: no  MOV: no
      R 6.5 n3b n2b calcCurr: no  MOV: no
      R 6.5 n3c n2c calcCurr: no  MOV: no
      L 345 n2a n1a calcCurr: no  MOV: no
      L 345 n2b n1b calcCurr: no  MOV: no
      L 345 n2c n1c calcCurr: no  MOV: no
      C 66.0 n6a n8a calcCurr: no  MOV: yes 250000
      C 66.0 n6b n8b calcCurr: no  MOV: yes 250000
      C 66.0 n6c n8c calcCurr: no  MOV: yes 250000
      C 66.0 n7a n8a calcCurr: no  MOV: yes 250000
      C 66.0 n7b n8b calcCurr: no  MOV: yes 250000
      C 66.0 n7c n8c calcCurr: no  MOV: yes 250000
      L 31.11 NodBa n10a calcCurr: no  MOV: no
      L 31.11 NodBb n10b calcCurr: no  MOV: no
      L 31.11 NodBc n10c calcCurr: no  MOV: no
      R 56.0 n10a GROUND calcCurr: no  MOV: no
      R 56.0 n10b GROUND calcCurr: no  MOV: no
      R 56.0 n10c GROUND calcCurr: no  MOV: no

   .END LUMPED
   .BEGIN LINES
      .BEGIN LINE-0
         phases: 6
         MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n1a no n4a no n1b no n4b no n1c no n4c no
                n1a no n5a no n1b no n5b no n1c no n5c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-0
      .BEGIN LINE-1
         phases: 6
         MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n4a no n6a no n4b no n6b no n4c no n6c no
                n5a no n7a no n5b no n7b no n5c no n7c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-1
      .BEGIN LINE-2
         phases: 3
         MmLink: 0
         Zc: 621.9 275.3 290.9
         delay: 0.4710e-3  0.3416e-3  0.3399e-3
         nodes: n8a no NodBa no n8b no NodBb no n8c no NodBc no
         q-matrix:
            0.58702696 -0.40302458  0.70710678
            0.55427582  0.82086139  0.00000000
            0.58702696 -0.40302458 -0.70710678
      .END LINE-2
      .BEGIN LINE-3
         phases: 3
         MmLink: 1
         Zc: 621.9 275.3 290.9
         delay: 0.4710e-3  0.3416e-3  0.3399e-3
         nodes: NodBa no GUNO no NodBb no GDOS no NodBc no GTRES no
         q-matrix:
            0.58702696 -0.40302458  0.70710678
            0.55427582  0.82086139  0.00000000
            0.58702696 -0.40302458 -0.70710678
      .END LINE-3
   .END LINES
   .BEGIN SOURCES
      408248   0 n3a
      408248  120 n3b
      408248 -120 n3c
   .END SOURCES
   .BEGIN SWITCHES
      total: 3
      n5a GROUND close: 1 open: 1
         close: 3000
         open: 3600

      n5b GROUND close: 1 open: 1
         close: 3000
         open: 3600

      n5c GROUND close: 1 open: 1
         close: 3000
         open: 3600
   .END SWITCHES
   .BEGIN OUTPUT
      NodBa NodBb NodBc
   .END OUTPUT
   .BEGIN DACS
      total: 3
      .BEGIN T0
         type: CCVT
         port: 0
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t0
      .BEGIN T1
         type: CCVT
         port: 1
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t1
      .BEGIN T2
         type: CCVT
         port: 2
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
   .END DACS
.END FILE
```

Test Case 1b

```
.BEGIN FILE
   .BEGIN GENERAL-DATA
      deltaT: 50.0E-6
      totalTime: 30000
      numLumped: 12
      numLines: 3
      numSources: 3
      numOutNodes: 3
   .END GENERAL-DATA
   .BEGIN LUMPED
      R 6.5 n3a n2a calcCurr: no  MOV: no
      R 6.5 n3b n2b calcCurr: no  MOV: no
      R 6.5 n3c n2c calcCurr: no  MOV: no
      L 345 n2a n1a calcCurr: no  MOV: no
      L 345 n2b n1b calcCurr: no  MOV: no
      L 345 n2c n1c calcCurr: no  MOV: no
      C 66.0 n6a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n6b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n6c NodAc calcCurr: no  MOV: yes 250000
      C 66.0 n7a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n7b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n7c NodAc calcCurr: no  MOV: yes 250000
   .END LUMPED
   .BEGIN LINES
      .BEGIN LINE-0
         phases: 6
         MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n1a no n4a no n1b no n4b no n1c no n4c no
                n1a no n5a no n1b no n5b no n1c no n5c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-0
      .BEGIN LINE-1
         phases: 6
         MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n4a no n6a no n4b no n6b no n4c no n6c no
                n5a no n7a no n5b no n7b no n5c no n7c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-1
      .BEGIN LINE-2
         phases: 3
         MmLink: 1
         Zc: 621.9 275.3 290.9
         delay: 0.4710e-3  0.3416e-3  0.3399e-3
         nodes: NodAa no GUNO no NodAb no GDOS no NodAc no GTRES no
         q-matrix:
            0.58702696 -0.40302458  0.70710678
            0.55427582  0.82086139  0.00000000
            0.58702696 -0.40302458 -0.70710678
      .END LINE-2
   .END LINES
   .BEGIN SOURCES
      408248   0 n3a
      408248  120 n3b
      408248 -120 n3c
   .END SOURCES
   .BEGIN SWITCHES
      total: 3
      GROUND n5a close: 1 open: 1
         close: 0.10
         open: 0.20

      GROUND n5b close: 1 open: 1
         close: 3000
         open: 3600

      GROUND n5c close: 1 open: 1
         close: 3000
         open: 3600
   .END SWITCHES
   .BEGIN OUTPUT
      NodAa NodAb NodAc
   .END OUTPUT
   .BEGIN DACS
      total: 3
      .BEGIN T0
         type: CCVT
         port: 0
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
```

```
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t0
      .BEGIN T1
         type: CCVT
         port: 1
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t1
      .BEGIN T2
         type: CCVT
         port: 2
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t2
   .END DACS
.END FILE
```

Test Case 2b[1]

```
.BEGIN FILE
   .BEGIN GENERAL-DATA
      deltaT: 40.0E-6
      totalTime: 30000
      numLumped: 12
      numLines: 3
      numSources: 3
      numOutNodes: 1
   .END GENERAL-DATA
   .BEGIN LUMPED
      R 6.5 n2a n1a calcCurr: no  MOV: no
      R 6.5 n2b n1b calcCurr: no  MOV: no
      R 6.5 n2c n1c calcCurr: no  MOV: no
      L 345 n1a n0a calcCurr: no  MOV: no
      L 345 n1b n0b calcCurr: no  MOV: no
      L 345 n1c n0c calcCurr: no  MOV: no
      C 66.0 n3a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n3b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n3c NodAc calcCurr: no  MOV: yes 250000
      C 66.0 n4a NodAa calcCurr: no  MOV: yes 250000
      C 66.0 n4b NodAb calcCurr: no  MOV: yes 250000
      C 66.0 n4c NodAc calcCurr: no  MOV: yes 250000
   .END LUMPED
   .BEGIN LINES
      .BEGIN LINE-0
         phases: 6
         MmLink: 0
         Zc: 987.9 328.4 275.9 222.6 237.2 244.1
         delay: 1.4069e-3    0.8699e-3   0.8506e-3
                0.8418e-3    0.8418e-3   0.8420e-3
         nodes: n0a no n3a no n0b no n3b no n0c no n3c no
                n0a no n4a no n0b no n4b no n0c no n4c no
         q-matrix:
            0.51146427 -0.48902472 -0.55148454  0.23244529 -0.41893693 -0.28289203
            0.33293163  0.01379915 -0.39499073 -0.48191931  0.26900888  0.58057410
            0.35712111  0.51054438 -0.16496383  0.45421967  0.48894408 -0.28793145
            0.35712111  0.51054438  0.16496383 -0.45421967 -0.48894408 -0.28793145
            0.33293163  0.01379915  0.39499073  0.48191931 -0.26900888  0.58057410
            0.51146427 -0.48902472  0.55148454 -0.23244529  0.41893693 -0.28289203
      .END LINE-0
      .BEGIN LINE-1
         phases: 3
         MmLink: 1
         Zc: 621.9 275.3 290.9
         delay: 0.4710e-3  0.3416e-3  0.3399e-3
         nodes: NodAa no GUNO no NodAb no GDOS no NodAc no GTRES no
         q-matrix:
```

[1] Case with two line links

```
            0.58702696 -0.40302458  0.70710678
            0.55427582  0.82086139  0.00000000
            0.58702696 -0.40302458 -0.70710678
      .END LINE-1
      .BEGIN LINE-2
         phases: 3
         MmLink: 2
         Zc: 621.9 275.3 290.9
         delay: 0.4710e-3  0.3416e-3  0.3399e-3
         nodes: NodAa no GUNO no NodAb no GDOS no NodAc no GTRES no
         q-matrix:
            0.58702696 -0.40302458  0.70710678
            0.55427582  0.82086139  0.00000000
            0.58702696 -0.40302458 -0.70710678
      .END LINE-2
   .END LINES
   .BEGIN SOURCES
      408248   0 n2a
      408248  120 n2b
      408248 -120 n2c
   .END SOURCES
   .BEGIN SWITCHES
      total: 0
   .END SWITCHES
   .BEGIN OUTPUT
      NodAa
   .END OUTPUT
   .BEGIN DACS
      total: 1
      .BEGIN T0
         type: CCVT
         port: 0
         C1: 9.97E-08   C2: 3.00E-10
         Cc: 1.30E-10   Lc: 0.708   Rc: 628
         Rf: 37.5       Lf: 0.73    Cf: 9.6E-06
         R: 100
         ratioa: 5000   ratiob: 110
      .END t0
   .END DACS
.END FILE
```

Real Time Input File[2]

Test Case 1a

```
.BEGIN FILE
   .BEGIN GENERAL-DATA
      initConditions: no
      totalTime:  3.000000000e+004
      deltaT:  4.990019960e-005
      lumped: 18
      lines: 4
      3ph-blocks: 1
      6ph-blocks: 3
      9ph-blocks: 1
      12ph-blocks: 0
      15ph-blocks: 0
      sources: 3
   .END GENERAL-DATA
   .BEGIN NODES
      1    n3a  2    n3b  3    n3c  4    n1a  5    n4a  6    n1b
      7    n4b  8    n1c  9    n4c  10    n5a  11    n5b  12    n5c  13    n6a
      14    n6b  15    n6c  16    n7a  17    n7b  18    n7c  19    n8a  20  NodBa
      21    n8b  22  NodBb  23    n8c  24  NodBc  25   GUNO  26   GDOS  27  GTRES
      28    n2a  29    n2b  30    n2c  31   n10a  32   n10b  33   n10c
   .END NODES
   .BEGIN BLOCKS
      .BEGIN BLOCK-30
         size: 3
         sources: no
         nodes:
          25   GUNO  26   GDOS  27  GTRES
         numSwStatus: 1
```

[2] Only Tesis Case 1a RTDNS input file is shown

```
         initSwStatus: 0
         A:
         switchStatus: 0
          3.98585768052983550e+002
          1.16776794444526690e+002 3.93826596145230500e+002
          1.07685767076704830e+002 1.16776794444526670e+002 3.98585768052983500e+002

      .END BLOCK-30
      .BEGIN BLOCK-60
         size: 6
         sources: yes
         nodes:
          28    n2a  4    n1a  6    n1b  8    n1c  29    n2b  30    n2c
          1    n3a  2    n3b  3    n3c
         shots: 334
         numSwStatus: 1
         initSwStatus: 0
         A:
         switchStatus: 0
          6.49699865385394750e+000
          1.12165735520932090e-001 2.38724923349250280e+002
          5.96027514653236780e-002 1.26853911391759140e+002 2.54664140164076660e+002
          5.71927667756561430e-002 1.21724685361708410e+002 1.26853911391759210e+002
2.38724923349250360e+002
        0.00000000000000000e+000 5.96027514653236710e-002 1.19654831977974570e-001 5.96027514653236920e-
002 6.49700217263196400e+000
        0.00000000000000000e+000 5.71927667756561430e-002 5.96027514653237190e-002 1.12165735520932130e-
001 0.00000000000000000e+000 6.49699865385394660e+000

         Gab:
         -1.53846e-001 0.00000e+000 0.00000e+000
          0.00000e+000 0.00000e+000 0.00000e+000
          0.00000e+000 0.00000e+000 0.00000e+000
          0.00000e+000 0.00000e+000 0.00000e+000
          0.00000e+000-1.53846e-001 0.00000e+000
          0.00000e+000 0.00000e+000-1.53846e-001

         sources:
           4.08248e+005          0.00  n3a
           4.08248e+005        120.00  n3b
           4.08248e+005       -120.00  n3c
      .END BLOCK-60
      .BEGIN BLOCK-61
         size: 6
         sources: no
         nodes:
          5    n4a  7    n4b  9    n4c  10    n5a  11    n5b  12    n5c
         numSwStatus: 8
         initSwStatus: 0
         A:
         switchStatus: 0
          1.90167503452413290e+002
          7.04866426837186280e+001 1.97657212577195200e+002
          5.48146643140818670e+001 7.51762535182828340e+001 2.00758557055152380e+002
          5.00904767326908950e+001 6.21942973234862540e+001 7.64400398359593250e+001
2.00758557055152410e+002
          5.80571208401811490e+001 6.45009165784957050e+001 6.21942973234862390e+001
7.51762535182828200e+001 1.97657212577195200e+002
          6.90018318131449320e+001 5.80571208401811700e+001 5.00904767326908950e+001
5.48146643140818740e+001 7.04866426837186420e+001 1.90167503452413310e+002

         switchStatus: 1
          1.77669625921748660e+002
          5.49687885574195430e+001 1.78389637255364450e+002
          3.57424110910364160e+001 5.14953970969511660e+001 1.71653547655638530e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000
          3.93001899628889360e+001 4.12115767288503460e+001 3.35704822395939710e+001
0.00000000000000000e+000 1.69506636203543740e+002
          5.53252408488032050e+001 4.10757299592906760e+001 2.92194603973220910e+001
0.00000000000000000e+000 4.99606877185066980e+001 1.75201030949624570e+002

         switchStatus: 2
          1.73114600417392550e+002
          5.15410273971645980e+001 1.76608811736061090e+002
          3.65465637565594080e+001 5.48805651848575380e+001 1.81188663454373680e+002
          2.80092342730034010e+001 3.76622441105388650e+001 5.27852781299789410e+001
1.72166283495502030e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000
```

```
          4.82980513714922490e+001 3.50554150063242390e+001 2.79113356062652260e+001
2.80060209513998900e+001 0.00000000000000000e+000 1.65031224679475430e+002

         switchStatus: 3
          1.68557859174961750e+002
          4.54138659279058100e+001 1.68370005608385840e+002
          2.79590796610056530e+001 4.33335189803903660e+001 1.65004974460866260e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000
          4.37418328950511470e+001 2.89289564673964070e+001 1.93248366982355190e+001
0.00000000000000000e+000 0.00000000000000000e+000 1.60475528909050410e+002

         switchStatus: 4
          1.65130350904628100e+002
          4.94207527969532590e+001 1.79932684363599290e+002
          3.66394525234181430e+001 5.98838991053753200e+001 1.87564631627530080e+002
          3.02011045779959910e+001 4.54596737304864930e+001 6.20017545475275330e+001
1.84958552483827990e+002
          3.24812081566964610e+001 4.29817218811148650e+001 4.36279835673727230e+001
5.48588933637309280e+001 1.71530946487439820e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000

         switchStatus: 5
          1.60198939485787120e+002
          4.19978337592621360e+001 1.68759467943326030e+002
          2.65154466423013840e+001 4.46449199146468770e+001 1.66780420703799080e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000
          2.35235300538899810e+001 2.94983367656911710e+001 2.52382005840503790e+001
0.00000000000000000e+000 1.55259743341230400e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000

         switchStatus: 6
          1.58979688852542380e+002
          4.12817068466882160e+001 1.69162450457143340e+002
          2.83780300528522820e+001 4.89517268395155580e+001 1.76468086140361550e+002
          1.98129899486405530e+001 3.17132930012326110e+001 4.80486869104154200e+001
1.67413624045427700e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000

         switchStatus: 7
          1.56634870305406620e+002
          3.75285167520683420e+001 1.63154976700353250e+002
          2.26915863346091630e+001 3.98498267104017150e+001 1.62677832647081540e+002
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000
          0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000
0.00000000000000000e+000 0.00000000000000000e+000 0.00000000000000000e+000

      .END BLOCK-61
      .BEGIN BLOCK-62
         size: 6
         sources: no
         nodes:
          20  NodBa  22  NodBb  24  NodBc  31   n10a  32   n10b  33   n10c
         numSwStatus: 1
         initSwStatus: 0
         A:
         switchStatus: 0
          1.69800896813590920e+002
          4.25952896594734090e+001 1.67743457332343240e+002
          3.89577705146050950e+001 4.25952896594734090e+001 1.69800896813590980e+002
          7.29828226442739680e+000 1.83080568420767050e+000 1.67445997603009980e+000
5.39067314162251850e+001
        1.83080568420767120e+000 7.20985061089727970e+000 1.83080568420767120e+000 7.86906129791195980e-
002 5.39029304989115370e+001
        1.67445997603010000e+000 1.83080568420767160e+000 7.29828226442740040e+000 7.19706537178657210e-
002 7.86906129791196530e-002 5.39067314162251990e+001

      .END BLOCK-62
      .BEGIN BLOCK-90
         size: 9
         sources: no
         nodes:
          13    n6a  14    n6b  15    n6c  16    n7a  17    n7b  18    n7c
          19    n8a  21    n8b  23    n8c
         numSwStatus: 1
         initSwStatus: 0
         A:
         switchStatus: 0
          1.48082042496012490e+002
          6.66765934059378790e+001 1.54344824666412190e+002
          6.39381644667309810e+001 6.66823415088062030e+001 1.48096876522046640e+002
          1.47711931687234740e+002 6.66820418062505380e+001 6.39423751249307840e+001
1.48096876522061820e+002
          6.66767843805432680e+001 1.53967339069060330e+002 6.66820418062457490e+001
6.66823415088109640e+001 1.54344824666412280e+002
          6.39340870019702120e+001 6.66767843805385070e+001 1.47711931687219590e+002
6.39381644667310030e+001 6.66765934059331610e+001 1.48082042495997430e+002
          1.47832483263018390e+002 6.66702433196850990e+001 6.39302844294020640e+001
1.47839897419550880e+002 6.66704884989597420e+001 6.39261410991537600e+001 1.47960631408367760e+002
          6.66667795629496710e+001 1.54087509455538480e+002 6.66722807507821640e+001
6.66722807507869390e+001 1.54087509455538510e+002 6.66667795629449240e+001 6.66604755062300280e+001
1.54207883485791650e+002
          6.39261410991537460e+001 6.66704884989549670e+001 1.47839897419535730e+002
6.39302844294020640e+001 6.66702433196803530e+001 1.47832483263003300e+002 6.39182455133034890e+001
6.66604755062252820e+001 1.47960631408352640e+002

      .END BLOCK-90
   .END BLOCKS
   .BEGIN OUTPUT
      numOutNodes: 3
       NodBa NodBb NodBc
      recordEveryOther: 1
   .END OUTPUT
   .BEGIN LUMPED
      R 6.50000e+000    n3a    n2a current: no  MOV: no
      R 6.50000e+000    n3b    n2b current: no  MOV: no
      R 6.50000e+000    n3c    n2c current: no  MOV: no
      L 3.45000e+002    n2a    n1a current: no  MOV: no
      L 3.45000e+002    n2b    n1b current: no  MOV: no
      L 3.45000e+002    n2c    n1c current: no  MOV: no
      C 6.60000e+001    n6a    n8a current: no  MOV: yes   2.50000000e+005
      C 6.60000e+001    n6b    n8b current: no  MOV: yes   2.50000000e+005
      C 6.60000e+001    n6c    n8c current: no  MOV: yes   2.50000000e+005
      C 6.60000e+001    n7a    n8a current: no  MOV: yes   2.50000000e+005
      C 6.60000e+001    n7b    n8b current: no  MOV: yes   2.50000000e+005
      C 6.60000e+001    n7c    n8c current: no  MOV: yes   2.50000000e+005
      L 3.11100e+001  NodBa   n10a current: no  MOV: no
      L 3.11100e+001  NodBb   n10b current: no  MOV: no
      L 3.11100e+001  NodBc   n10c current: no  MOV: no
      R 5.60000e+001   n10a GROUND current: no  MOV: no
      R 5.60000e+001   n10b GROUND current: no  MOV: no
      R 5.60000e+001   n10c GROUND current: no  MOV: no
   .END LUMPED
   .BEGIN LINES
      .BEGIN LINE-0
         phases: 6
         MmLink: 0
         delay: 1.4069e-003 8.6990e-004 8.5060e-004 8.4180e-004 8.4180e-004 8.4200e-004
         Zc:      987.90      328.40      275.90      222.60      237.20      244.10
         Q:
          5.1146427e-001 -4.8902472e-001 -5.5148454e-001 2.3244529e-001 -4.1893693e-001 -2.8289203e-001
          3.3293163e-001 1.3799150e-002 -3.9499073e-001 -4.8191931e-001 2.6900888e-001 5.8057410e-001
          3.5712111e-001 5.1054438e-001 -1.6496383e-001 4.5421967e-001 4.8894408e-001 -2.8793145e-001
          3.5712111e-001 5.1054438e-001 1.6496383e-001 -4.5421967e-001 -4.8894408e-001 -2.8793145e-001
          3.3293163e-001 1.3799150e-002 3.9499073e-001 4.8191931e-001 -2.6900888e-001 5.8057410e-001
          5.1146427e-001 -4.8902472e-001 5.5148454e-001 -2.3244529e-001 4.1893693e-001 -2.8289203e-001

         g:
          3.4058426e-003
          -7.0983944e-004 3.4075382e-003
          -3.0119034e-004 -7.3570212e-004 3.2957907e-003
          -1.8216425e-004 -3.5033407e-004 -7.7090140e-004 3.2957907e-003
          -3.3219722e-004 -4.2026982e-004 -3.5033407e-004 -7.3570212e-004 3.4075382e-003
         -7.6411917e-004 -3.3219722e-004 -1.8216425e-004 -3.0119034e-004 -7.0983944e-004 3.4058426e-003

         calcCurr:
          no no no no no no no no no no no no
         nodes:  n1a n4a  n1b n4b  n1c n4c  n1a n5a  n1b n5b  n1c n5c
      .END LINE-0
      .BEGIN LINE-1
         phases: 6
         MmLink: 0
         delay: 1.4069e-003 8.6990e-004 8.5060e-004 8.4180e-004 8.4180e-004 8.4200e-004
         Zc:      987.90      328.40      275.90      222.60      237.20      244.10
         Q:
          5.1146427e-001 -4.8902472e-001 -5.5148454e-001 2.3244529e-001 -4.1893693e-001 -2.8289203e-001
          3.3293163e-001 1.3799150e-002 -3.9499073e-001 -4.8191931e-001 2.6900888e-001 5.8057410e-001
          3.5712111e-001 5.1054438e-001 -1.6496383e-001 4.5421967e-001 4.8894408e-001 -2.8793145e-001
          3.5712111e-001 5.1054438e-001 1.6496383e-001 -4.5421967e-001 -4.8894408e-001 -2.8793145e-001
          3.3293163e-001 1.3799150e-002 3.9499073e-001 4.8191931e-001 -2.6900888e-001 5.8057410e-001
          5.1146427e-001 -4.8902472e-001 5.5148454e-001 -2.3244529e-001 4.1893693e-001 -2.8289203e-001

         g:
          3.4058426e-003
          -7.0983944e-004 3.4075382e-003
          -3.0119034e-004 -7.3570212e-004 3.2957907e-003
          -1.8216425e-004 -3.5033407e-004 -7.7090140e-004 3.2957907e-003
          -3.3219722e-004 -4.2026982e-004 -3.5033407e-004 -7.3570212e-004 3.4075382e-003
         -7.6411917e-004 -3.3219722e-004 -1.8216425e-004 -3.0119034e-004 -7.0983944e-004 3.4058426e-003

         calcCurr:
          no no no no no no no no no no no no
         nodes:  n4a n6a  n4b n6b  n4c n6c  n5a n7a  n5b n7b  n5c n7c
      .END LINE-1
      .BEGIN LINE-2
         phases: 3
         MmLink: 0
         delay: 4.7100e-004 3.4160e-004 3.3990e-004
         Zc:      621.90      275.30      290.90
         Q:
          5.8702696e-001 -4.0302458e-001 7.0710678e-001
          5.5427582e-001 8.2086139e-001 0.0000000e+000
          5.8702696e-001 -4.0302458e-001 -7.0710678e-001

         g:
          2.8629197e-003
          -6.7850268e-004 2.9415655e-003
          -5.7468770e-004 -6.7850268e-004 2.8629197e-003

         calcCurr:
          no no no no no no
         nodes:  n8a NodBa  n8b NodBb  n8c NodBc
      .END LINE-2
      .BEGIN LINE-3
         phases: 3
         MmLink: 1
         delay: 4.7100e-004 3.4160e-004 3.3990e-004
         Zc:      621.90      275.30      290.90
         Q:
          5.8702696e-001 -4.0302458e-001 7.0710678e-001
          5.5427582e-001 8.2086139e-001 0.0000000e+000
          5.8702696e-001 -4.0302458e-001 -7.0710678e-001

         g:
          2.8629197e-003
          -6.7850268e-004 2.9415655e-003
          -5.7468770e-004 -6.7850268e-004 2.8629197e-003

         calcCurr:
          no no no no no no
         nodes:  NodBa GUNO  NodBb GDOS  NodBc GTRES
      .END LINE-3
   .END LINES
   .BEGIN SWITCHES
      total: 3
      switch: 0 n5a GROUND
         initiallyClosed:  no  blk: 2  pos: 0  numGaLink: 2
         gaLink:  25 add: no   36 add: no
      switch: 1 n5b GROUND
         initiallyClosed:  no  blk: 2  pos: 1  numGaLink: 2
         gaLink:  27 add: no   38 add: no
      switch: 2 n5c GROUND
         initiallyClosed:  no  blk: 2  pos: 2  numGaLink: 2
         gaLink:  29 add: no   40 add: no
      events: 6
        t: 3.00e+003  sw: 0  openOperation:  no
        t: 3.00e+003  sw: 1  openOperation:  no
        t: 3.00e+003  sw: 2  openOperation:  no
        t: 3.60e+003  sw: 0  openOperation: yes
        t: 3.60e+003  sw: 2  openOperation: yes
        t: 3.60e+003  sw: 1  openOperation: yes
   .END SWITCHES
```

```
   .BEGIN DACS
      total: 3
      .BEGIN T0
         type: CCVT
         port: 0
         C1: 9.970000e-008
         C2: 3.000000e-010
         Cc: 1.300000e-010
         Lc: 7.080000e-001
         Rc: 6.280000e+002
         Rf: 3.750000e+001
         Lf: 7.300000e-001
         Cf: 9.600000e-006
         R:  1.000000e+002
         ratioa: 5.000000e+003
         ratiob: 1.100000e+002
      .END T0
      .BEGIN T1
         type: CCVT
         port: 1
         C1: 9.970000e-008
         C2: 3.000000e-010
         Cc: 1.300000e-010
         Lc: 7.080000e-001
         Rc: 6.280000e+002
         Rf: 3.750000e+001
         Lf: 7.300000e-001
         Cf: 9.600000e-006
         R:  1.000000e+002
         ratioa: 5.000000e+003
         ratiob: 1.100000e+002
      .END T1
      .BEGIN T2
         type: CCVT
         port: 2
         C1: 9.970000e-008
         C2: 3.000000e-010
         Cc: 1.300000e-010
         Lc: 7.080000e-001
         Rc: 6.280000e+002
         Rf: 3.750000e+001
         Lf: 7.300000e-001
         Cf: 9.600000e-006
         R:  1.000000e+002
         ratioa: 5.000000e+003
         ratiob: 1.100000e+002
      .END T2
   .END DACS
.END FILE
```