

Figure C.4: Address decoding and D/A schematic.

C.3 Software

Appendix E contains a listing of the 8088 assembly-language routine to read and write a block of samples to and from the analog interface board. The routine can be called from programs compiled with Microsoft FORTRAN version 3.3 or 4.0. The routine is passed an array of 16-bit numbers (declared with the LARGE attribute) and a 32-bit integer containing the number of samples to be read and written. The array may extend over multiple 64k segments. The routine sends the block of samples to the D/A and replaces these samples with the samples input from the A/D. The routine also converts the samples between two's-complement and the left-aligned unsigned format required by the hardware. The routines were only tested on an IBM PC AT although they were designed to work with an IBM PC as well.

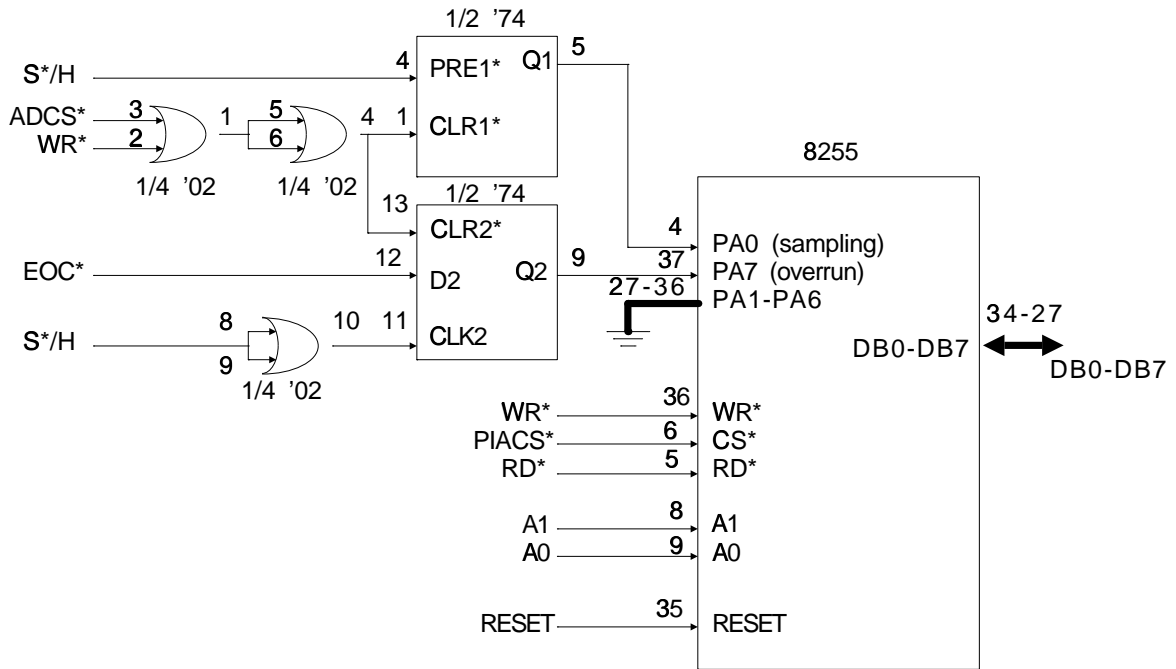


Figure C.3: A/D status circuit schematic.

pre-loaded into the D/A without changing the current output value. The new input value is transferred to the output on the next falling edge of the (hardware-generated) \bar{S}/H signal.

C.2.5 A/D and D/A Analog Interface

The D/A and A/D interfaces were designed to operate with signals between ± 2.5 volts. Shielded cable was used to reduce digital noise pickup and RF leakage. Ferrite beads were used to reduce RF output from the PC.

The D/A interface, shown in Figure C.5, supplies a ± 2.5 volt signal from the D/A. The 100 pF compensating capacitor was required to avoid oscillation with some loads.

The A/D analog interface, shown in Figure C.6, converts the input bipolar signal to a 0 to 5 volt signal. The input offset is adjustable. The A/D input is protected with diodes.

Since neither interface circuit includes filtering, the analog input and output signals were filtered using external Krohn-Hite model 3342 filters.

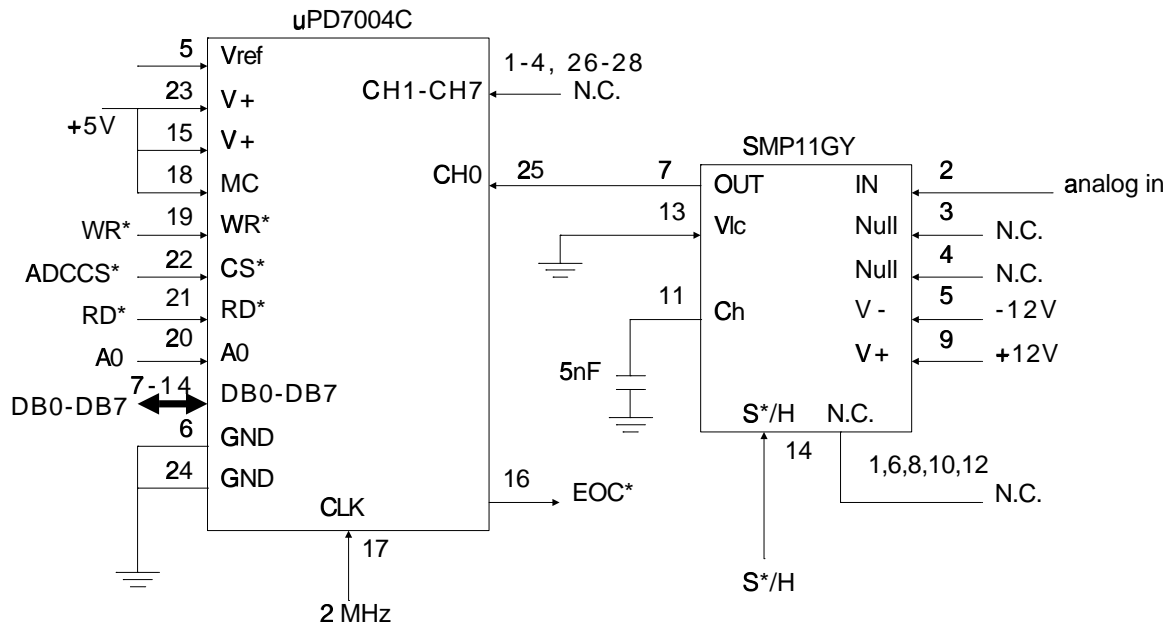


Figure C.2: A/D and sample-and-hold schematic.

indicates that an A/D overrun has occurred. This bit is set by latching the A/D's $\overline{\text{EOC}}$ (end of conversion) status signal into a second latch with the falling edge of the $\overline{\text{S/H}}$ control signal (start of sampling). This status signal is thus set if a conversion did not complete before the start of sampling for the next sample. Both status latches are cleared when the CPU starts a new conversion by writing to the A/D (indicated by $\overline{\text{ADCS}}$ and $\overline{\text{WR}}$ signals).

C.2.4 Address Decoding and D/A

Figure C.4 shows the address decoding circuitry that generates chip selects for the four I/O devices (NEC μPD7400 A/D, National 1208 D/A, 8253 timer and 8255 parallel interface) and the D/A. The remainder of the address decoding circuit was built into the prototyping board [81] and is not shown here.

The D/A is a National 1208LCD with 12-bit resolution and is linear to ± 0.012 percent of the full-scale output. The input registers are double buffered so that a value can be

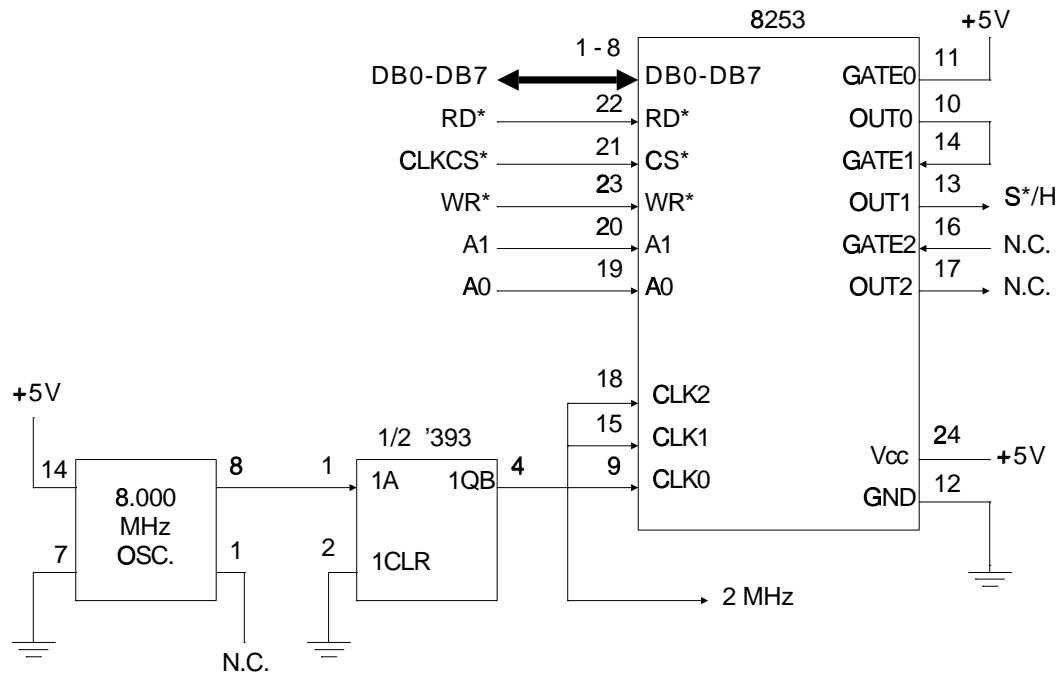


Figure C.1: Timing circuit schematic.

C.2.2 A/D

Figure C.2 shows the schematic of the A/D converter and the sample-and-hold circuits. The \bar{S}/H signal controls the PMI SMP-11GY sample-and-hold. The NEC μ PD7004 A/D converter chip has a conversion time of 100 microseconds, 10 bit resolution and ± 1 bit linearity. The A/D's clock rate and input channel (0) are selected by writing to registers in the chip. Conversions are started under program control by writing to a register.

C.2.3 A/D Status

Figure C.3 shows the circuit that lets the CPU test the A/D status and check for overruns. The 8255 parallel interface chip reads the "sampling" and "overrun" status latches. The "sampling" signal indicates that the \bar{S}/H is in sampling mode and thus that the previous conversion should have completed. When this signal goes high the CPU reads the A/D result and starts another conversion by writing to the A/D. The "overrun" status bit

Appendix C

The Analog/Digital Interface

C.1 Introduction

This appendix describes the analog interface board that was built to generate and sample the baseband OFDM signal. The interface features an 8 kHz sampling rate with simultaneous input and output sampling, no sampling jitter, and a reliable error indication for any sampling overrun condition. The interface was also used to measure the statistics of the fading simulator described in Appendix B. The interface circuit was built on an IBM PC wire-wrap prototyping board [81].

C.2 Circuit Description

C.2.1 Timer Circuit

Figure C.1 shows the schematic of the timing circuit. The hardware and software support a maximum sampling rate of 8 kHz. An 8 MHz crystal oscillator clock is divided by 4 to produce a 2 MHz timing clock. The 8253 timer generates the master timing signal labelled \overline{S}/H (sample and hold). Two of the 8253's programmable timer sections are used. Section 0 of the timer divides the 2 MHz clock to generate an 8 kHz clock. Section 1 of the timer is a one-shot triggered from the 8 kHz clock and generates \overline{S}/H , a $4\mu\text{s}$ -long pulse every $125\ \mu\text{s}$.

B.4.2 Level Crossing Rate

The LCR measurements check time statistics. Figure B.13 compares the theoretical and measured LCRs for Doppler rates of 2, 20, and 120 Hz. The 2 Hz measurements were made on every tenth sample to reduce spurious level crossings caused by noise. The 2 Hz measurements are thus based on only 100,000 samples. The LCR measurements generally agree with the theoretical values for levels from -30 to $+10$ dB (± 1 dB).

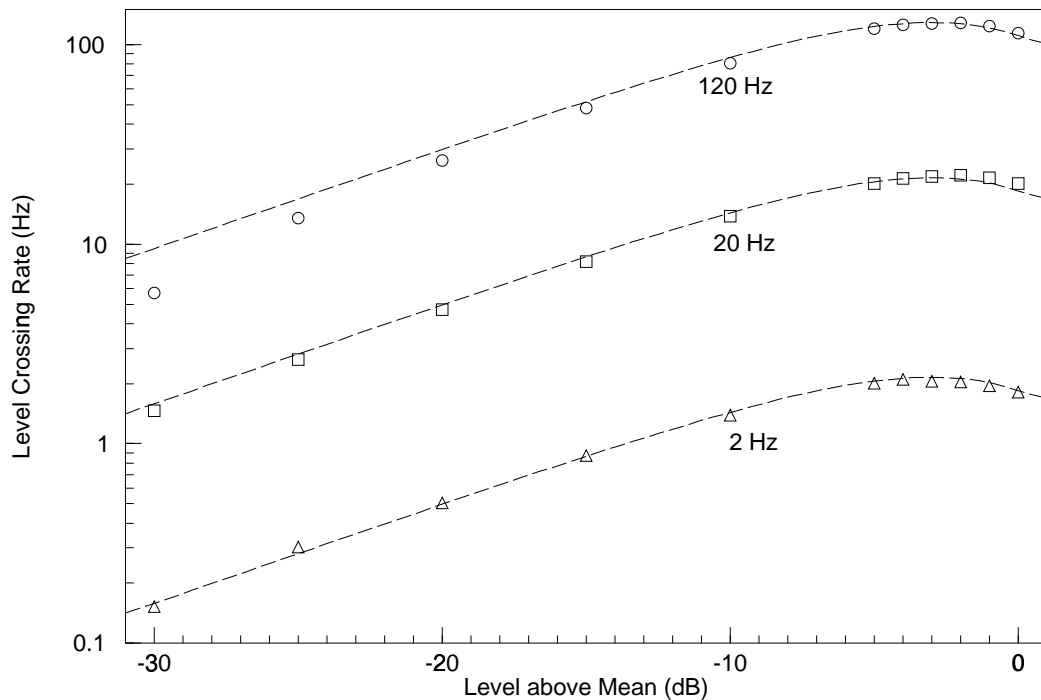


Figure B.13: Comparison of theoretical and measured level crossing rates (LCRs) for three Doppler frequencies. The deviations from the theoretical at 120 Hz are due to limitations of the measurement method.

For some of the 120 Hz LCR measurements the sampling period is on the order of the average fade duration so many level crossings are not detected. The measurements are therefore lower than expected. For example, at a Doppler rate of 120 Hz the average fade duration at -30 dB is $105 \mu\text{s}$ while the sampling period is $125 \mu\text{s}$.

signal was sampled with a 10-bit A/D converter (see Appendix C) at 8 kHz. The LCR and CPDF were computed from one million samples (approximately 2 minutes sampling time). Similar results were obtained using the IC2AT transmitter as the signal source.

B.4.1 CPDF

The CPDF measurements test the distribution of the envelope level and the simulator's dynamic range. Figure B.12 compares the Rayleigh CPDF and the measured CPDFs for Doppler rates of 2, 20, and 120 Hz. The measured distributions are Rayleigh to within about 1 dB between -40 to $+10$ dB.

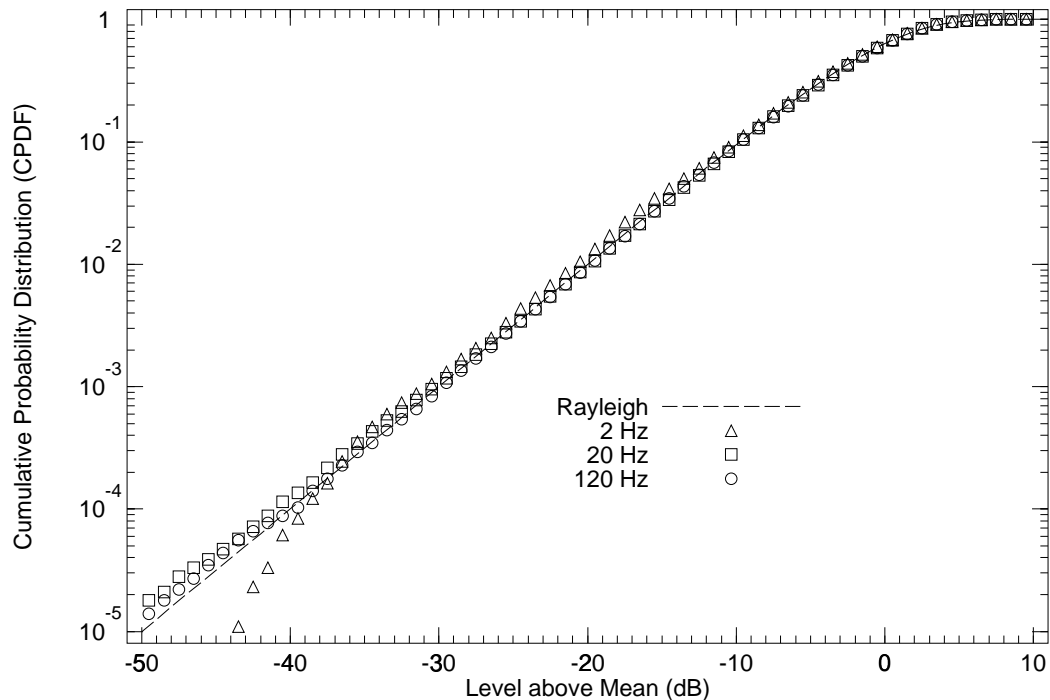


Figure B.12: Comparison of measured and Rayleigh CPDFs (cumulative probability distribution functions) for three Doppler rates. The CPDF is the probability that the signal will be below the indicated level.

connectors was used. Aluminum foil was used as a gasket to seal the aluminum box. Connections to the signal source were made with well-shielded co-ax cable.

B.4 Performance Measurements

The simulator was tested by measuring the cumulative probability distribution function (CPDF) and the level crossing rate (LCR) (see Section 2.1). Figure B.11 shows how the measurements were made.

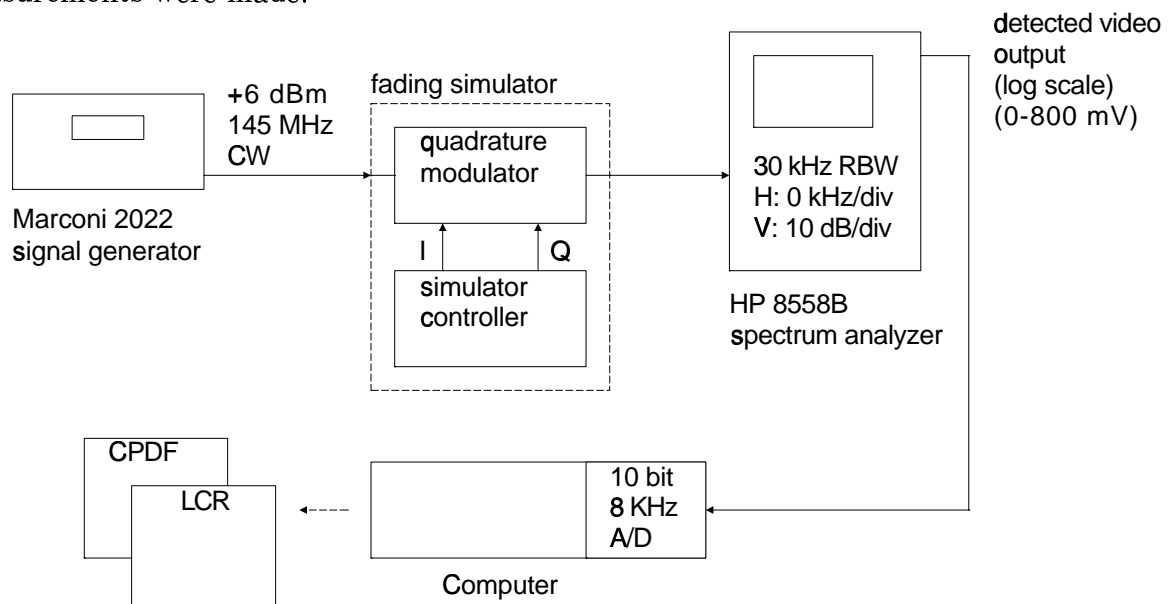


Figure B.11: Fading simulator performance measurement setup. The detected video signal from the spectrum analyzer is proportional to the signal level in dB. This signal is digitized and the computer then calculates various statistics to confirm proper operation.

The Marconi 2022 signal generator produced a +6 dBm CW signal (the maximum generator output) at 145 MHz. An HP 8558B spectrum analyzer measured the level of the simulator output. The frequency sweep was set to zero so that the spectrum analyzer operated as a frequency-selective envelope detector. A 30 kHz resolution bandwidth (RBW) with no video filtering was used to avoid distorting the envelope waveform. The 8558B provides an analog voltage output proportional to the signal level in dB. This

B.3.2 IF Port Network

The mixers require 50 ohm terminations at all three ports. A 50 ohm resistor in series with a 1 nF DC-blocking capacitor provides the proper termination at the IF port. The 590 ohm current-limiting resistor converts the control signal voltage to a current for the (current-controlled) mixer. The ferrite bead and the 1 nF bypass capacitor help reduce RF leakage through the control unit. The bandwidth of this network is much greater than that of the control signal.

The rise time of the mixer output was measured with a spectrum analyzer used as an envelope detector (Section B.4).

B.3.3 Splitters

One of the two Merrimac 113A in-phase (0°) -3 dB power splitters is used as a power splitter, the other as a combiner (see Figure B.10). The amplitude imbalance between the branches was measured to be less than 0.1 dB and the phase imbalance less than 2° .

B.3.4 Delay Line

The 90° phase shift is produced by making one of the co-ax cable connections an electrical quarter-wavelength longer than the other. Performance should be equally good within a few percent of the center frequency even though the phase shift is exactly 90° at only one frequency. The design center frequency was 145.5 MHz.

B.3.5 Construction

The components were mounted on an insulating board and connected with short pieces of thin, well-shielded co-ax cable (RG-316/U). Good shielding is required to prevent signal leaks from forming a path around the fading simulator. Such paths prevent deep fades and reduce the dynamic range of the simulator. A cast aluminum box with BNC

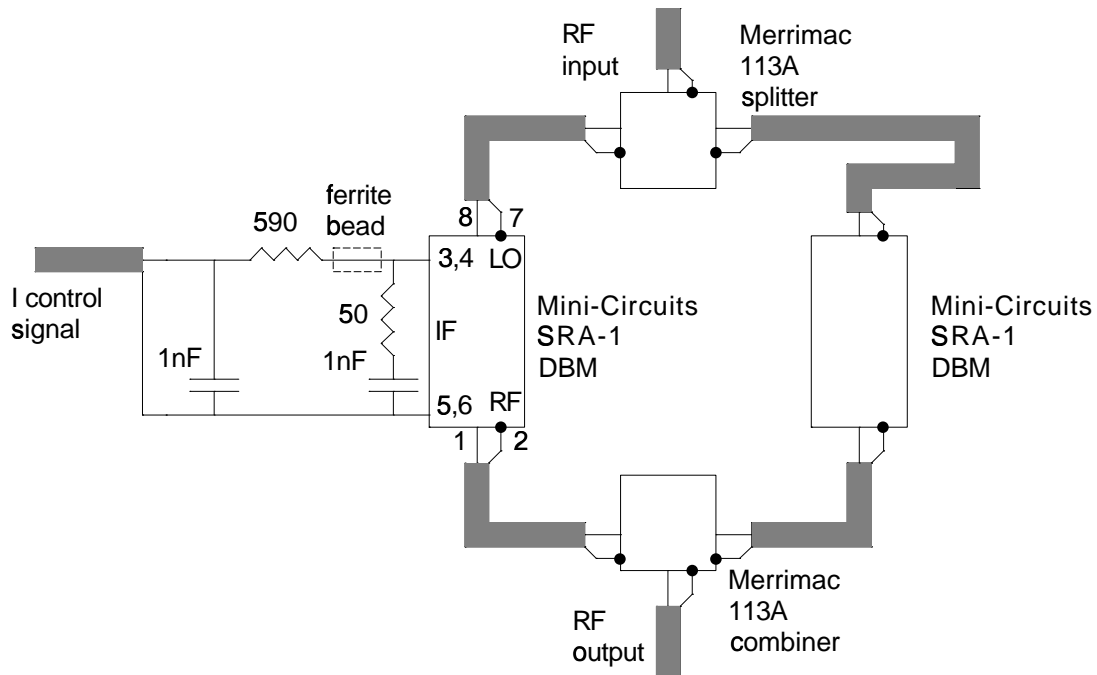


Figure B.10: Diagram of the RF quadrature modulator with schematic of the IF port matching network. Only one of the two matching networks is shown.

RF output will not be a linear function of the control current. The input to the fading simulator should be approximately 11 dBm since the loss between the power splitter input and each output is about 3.8 dB. More information on mixer selection is available in [66]. Either the RF or LO port can be used as the RF input. The control signal must be applied at the DC-coupled IF port.

A lower RF drive level would be desirable to reduce the amount of RF leakage and the shielding requirements. A version of the control unit was built using a look-up table to make the mixer attenuation a linear function of control current at reduced RF drive levels. The fading had the right amplitude distribution but the wrong level crossing rate (see Section B.4). This is believed to result from control current effects on the mixer phase shifts.

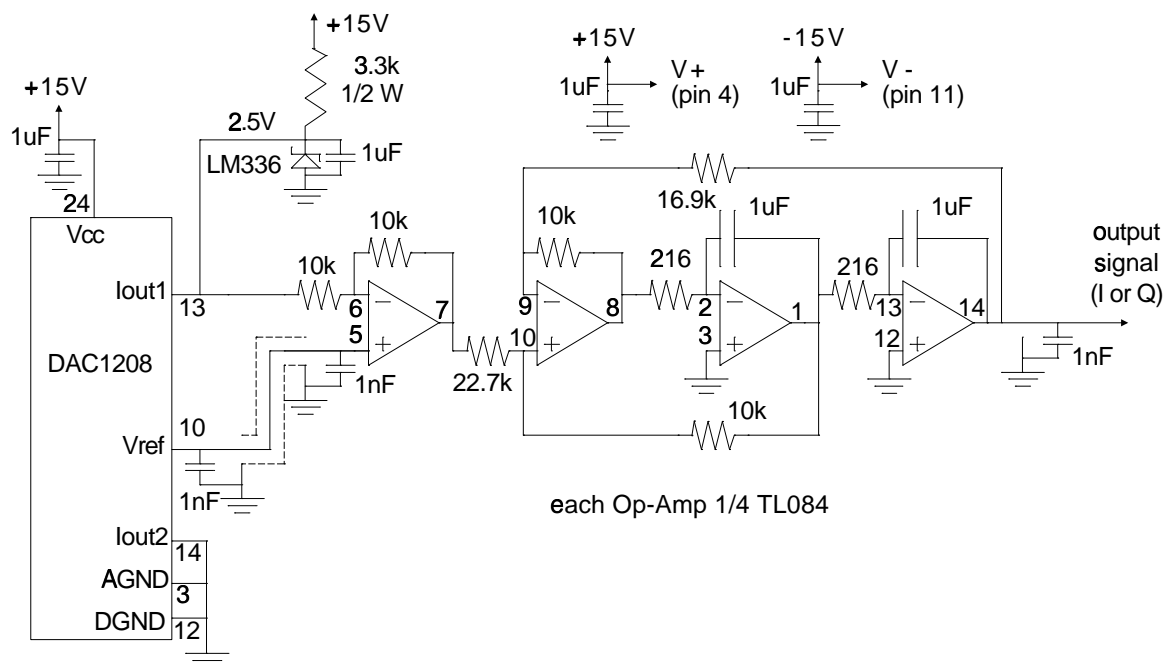


Figure B.9: Analog interface schematic. One of two reconstruction filters is shown.

Construction

The prototype was built with 3M ScotchflexTM push-wire sockets. These sockets sped up the wiring but cost more than wire-wrap sockets. A ground plane was not used but it may have reduced the amount of digital noise.

B.3 The RF Quadrature Modulator

Figure B.10 shows the components in the quadrature modulator and the IF port matching network. The unit described here operates at 145 MHz although wideband units can also be built or bought.

B.3.1 Mixers

The RF drive level to the mixers is critical. The RF drive level to the Mini-Circuits SRA-1 double-balanced mixers must be sufficiently high (approximately +7 dBm) or the

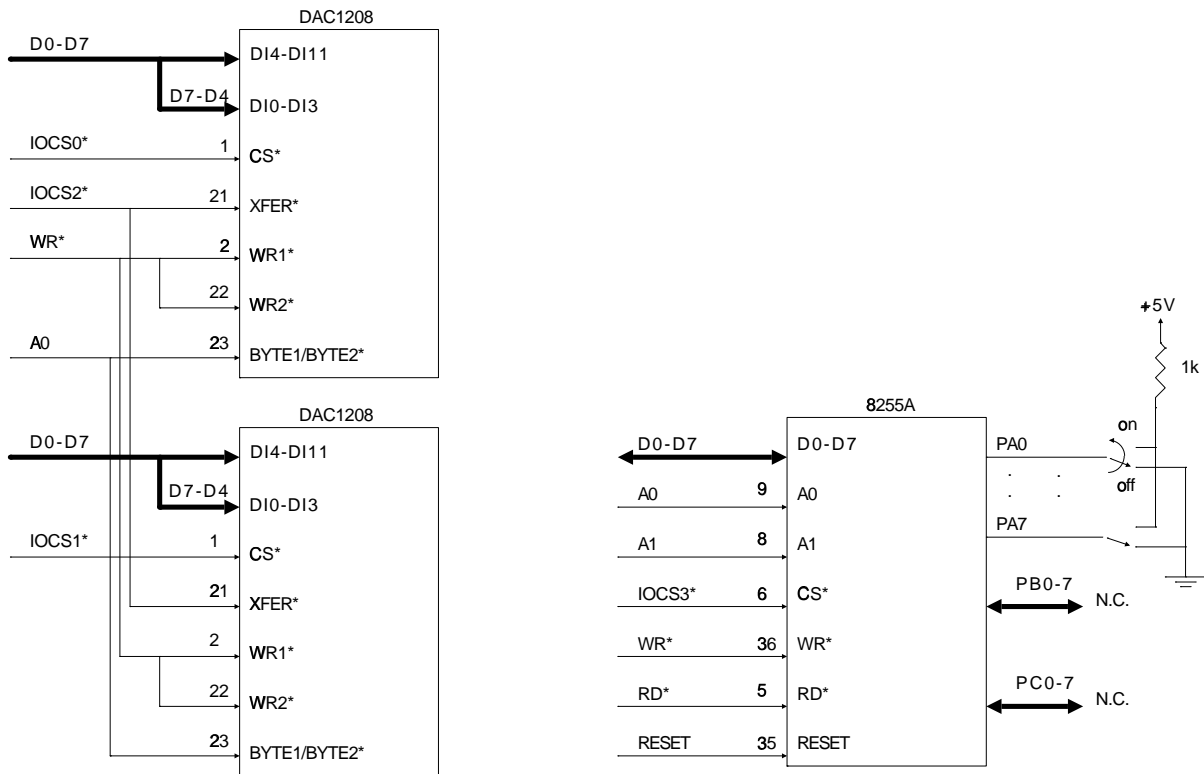


Figure B.8: D/A and parallel I/O schematic.

are used for the filter and one is used to convert the 0 to 5 volt D/A output to ± 2.5 volts.

The major sources of noise on the control signals were digital signal noise coupling onto the analog circuitry and D/A switching transients. The digital and analog circuits used separate power and return lines to reduce the effect of the digital signal noise. A 47 nF capacitor (not shown on the schematics) was also connected from the power supply line to ground near each logic IC. Ringing at the D/A output transitions was reduced by using a low-impedance return (the chassis) for connections between the D/A and the analog circuit (on a separate board). In addition, the D/A output was bypassed to ground by small (1 nF) capacitors to filter out the highest frequency components. These steps reduced the output noise level to less than 2 mV.

The design could be improved by using a sample-and-hold on the output of the D/A to let the D/A switching transients die out before the sample is output.

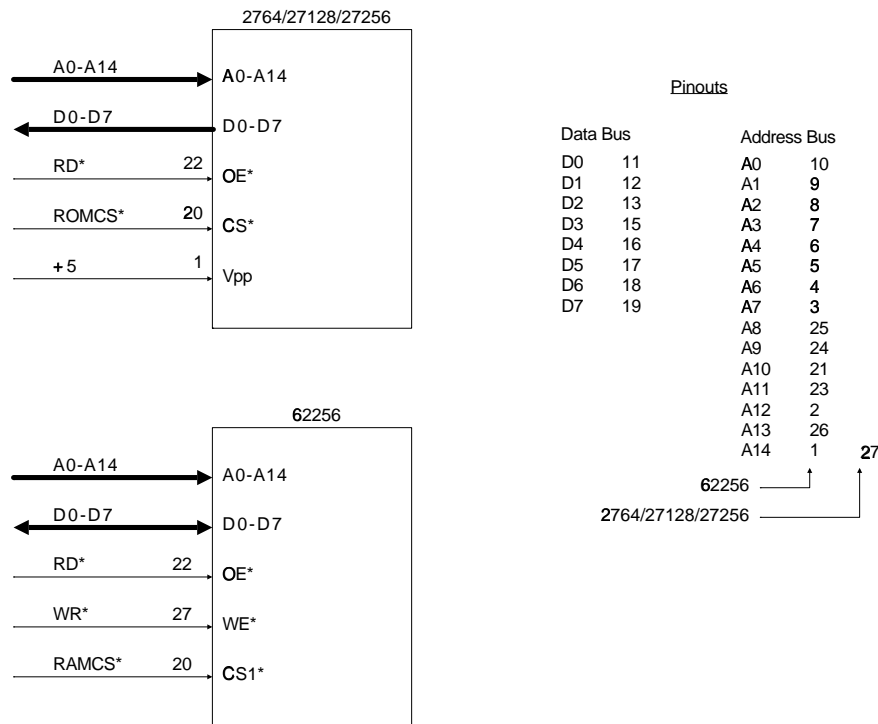


Figure B.7: Memory schematic.

The filter's cut-off frequency must be greater than the maximum Doppler rate while still providing enough filtering at the lowest effective sampling rate. The filter must also have a linear phase response up to the maximum Doppler frequency because a non-linear phase response would change the phase relationships between the control signal frequency components. Although a high- Q filter has a more linear phase over the pass-band it also has a poor transient response to step changes in D/A output. Finally, the gain of the filter must be high enough to let the D/A drive the mixers to minimum attenuation. A filter output of about 2 volts provides enough current to drive the quadrature modulator to minimum attenuation when used with the mixer interface circuit described in the next section.

A second-order Butterworth filter was selected. The 3 dB frequency is 570 Hz, the Q is 0.7, and the gain is 0.8. The schematic is given in Figure B.9. Three of the amplifiers

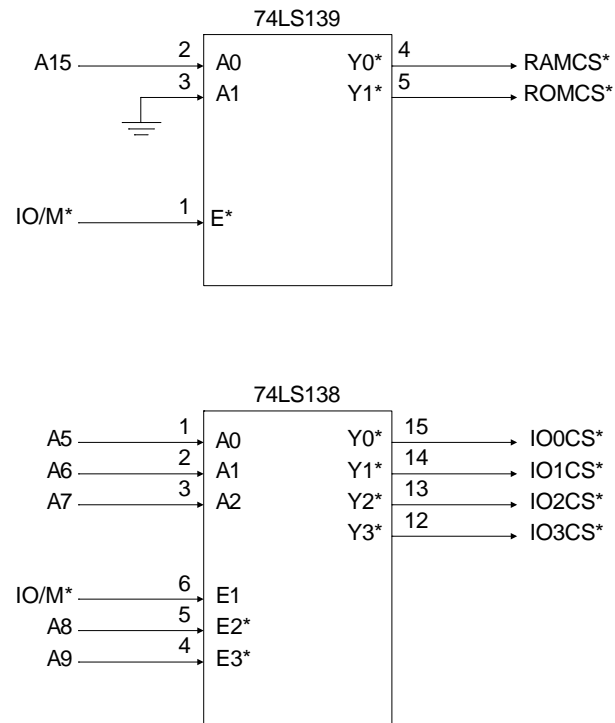


Figure B.6: Address decoding schematic.

contains the program and about 22k bytes of look-up tables.

Figure B.8 shows the D/A output circuit and the switch input circuit. One 8-bit port on the 8255A parallel interface chip reads the positions of the eight toggle switches. These switches set the simulator's run/stop status, the Doppler rate when the simulator is running, and the RF level when the simulator is stopped. The D/As are 12-bit National Semiconductor DAC1208LCD. Their double-buffered data registers allow values to be pre-loaded into each D/A and then output simultaneously using a common control signal.

Analog Section

The reconstruction filters create a continuous waveform from the discrete D/A output. A simple filter can be used because the sampling rate, approximately 3 kHz, is much higher than the maximum Doppler rate.

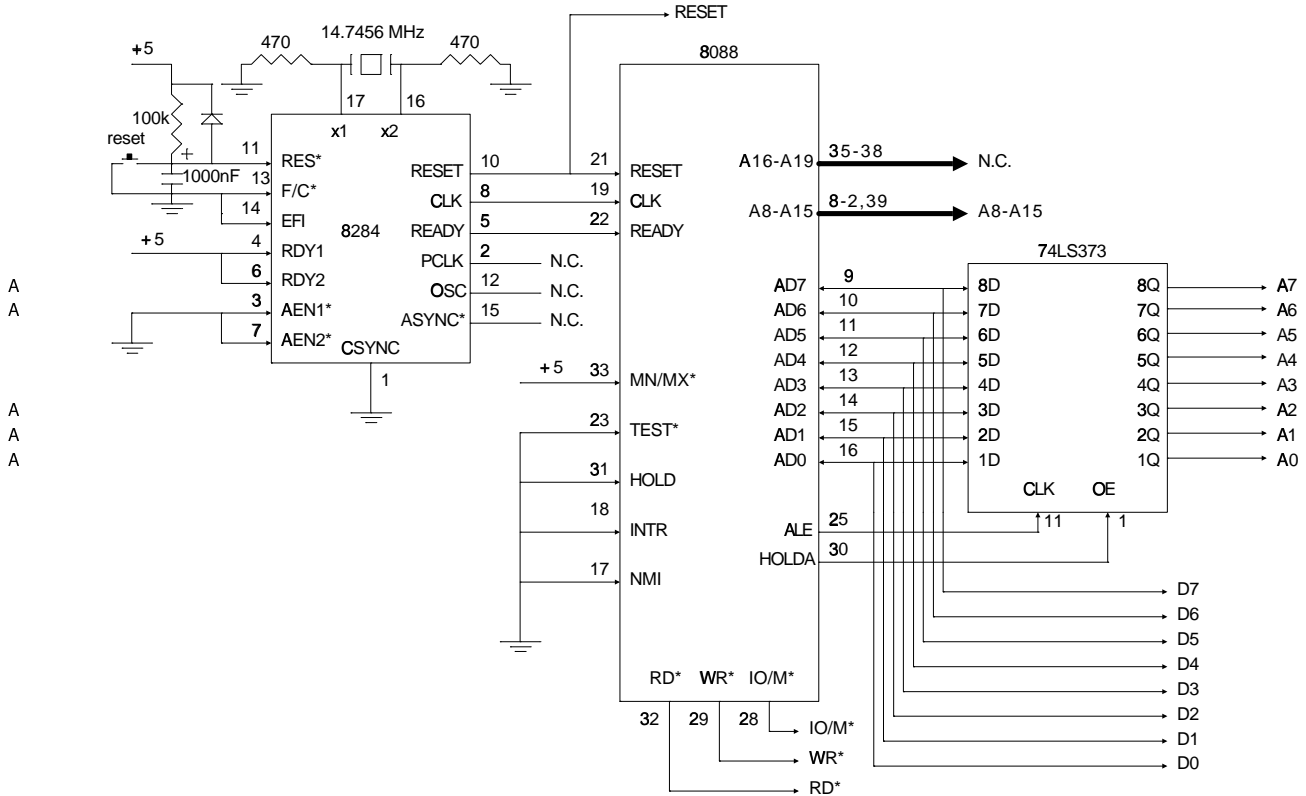


Figure B.5: CPU schematic.

The number of ICs required is about the same as for a design with an 8-bit CPU. The 8088 is easier to interface than other 8-bit processors because of more relaxed bus timing specifications. This allows the relatively slow D/As to be connected directly to the CPU bus. The 8284 clock chip provides a 5 MHz clock for the 8088 microprocessor. The 74LS373 demultiplexes the 8088's address/data bus.

Figure B.6 shows the memory and I/O address decoding circuits. A 74LS139 dual two-to-four decoder selects either the RAM or the EPROM. A 74LS138 three-to-eight decoder selects one of the two D/As, the parallel interface chip, or a common output transfer signal for the D/As.

Figure B.7 shows the two memory chips. A 32k static RAM (62256P-12) was used so that code could be downloaded to the control unit for testing. The 32k EPROM (27256-25)

be more than twice the reconstruction filter bandwidth, a larger cosine table size allows lower Doppler rates to be generated for a given reconstruction filter bandwidth.

Offsets are added to the 12 most significant bits of the **I** and **Q** control signal sums to convert from two's-complement to the offset-binary format required by the D/As. These offsets are the sample values that result in minimum RF output for a given mixer. These offsets do not necessarily produce a zero volt control signal. The offset values were measured by adjusting the D/A output to obtain minimum RF output. Finally, the two sample values are loaded into the D/As and output simultaneously.

The fading waveform will eventually repeat because each phase counter can only take on a finite number of discrete phases. The state of each counter is defined by its least significant 28 bits since these are the only bits used to compute the phase. Each counter is initialized to zero. The period of the fading waveform is therefore the number of samples until all of the counters again have their least significant 28 bits equal to zero.

The least significant 28 bits of a counter will return to zero when the counter reaches a multiple of 2^{28} . If p is the period, m is the counter increment, and i is an integer, then $pm = i2^{28}$ or $p = i\frac{2^{28}}{m}$. If m and 2^{28} have no common factors (for example, m is odd) then the smallest i that will make p an integer is $i = m$, giving $p = 2^{28}$. If they do have a common factor, the period will be 2^{28} divided by the largest common factor.

Since each oscillator has a period that is a factor of 2^{28} , the period of the fading waveform will be that of the oscillator with the longest period. A period of 2^{28} corresponds to about 25 hours at a $338 \mu\text{s}$ sample period.

B.2.2 Hardware Description

Digital Section

Figure B.5 shows the schematic of the CPU section. The 8088 microprocessor was chosen primarily because a development system, an IBM PC, was readily available. The 8088 is also slightly faster than 8-bit microprocessors because it has more 16-bit registers.

In this case the most significant bit selects a level of either 0 dB¹ (switch off), or -20 dB (switch on). The 0 dB level is used when measuring the mean signal level and the -20 dB level is used to check the calibration of the fading simulator attenuation. The control signal values that produce a 0 dB RF level are computed by summing the powers of the nine sinusoids.

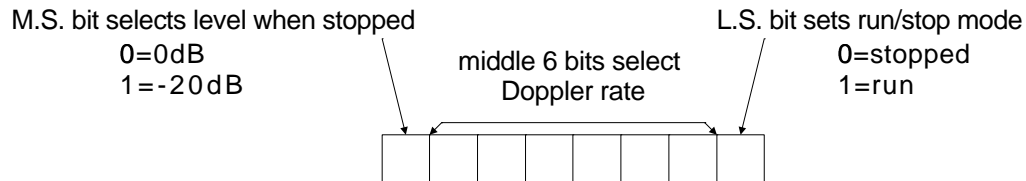


Figure B.4: Switch register bits.

The phase (0 to 2π) of each of the nine sinusoids is represented by a 32-bit integer. Each sinusoid's phase is incremented once per sample by an amount proportional to its frequency. The phase increments are retrieved from a 2304-byte table (64 Doppler rates \times 9 sinusoids \times 4 bytes). A listing of the FORTRAN program used to generate these tables is given in Appendix E. The phase counters and increments are scaled so that the least significant 12 bits of the most significant (16-bit) word of the phase count form a pointer into a scaled cosine table of 2048 (16-bit) words. The values looked up in these tables convert the phases to the oscillator outputs. The oscillator amplitudes are set by the scaling of the cosine tables. The values of the nine sinusoids obtained in this way are added to form the **I** and **Q** signals. A listing of the program used to generate these tables is given in Appendix E. One table is required for each of the five oscillator amplitudes. The five scaled cosine tables of 2048 16-bit values require 20k bytes.

The lowest Doppler rate that can be generated is determined by the length of the cosine table and the bandwidth of the reconstruction filter. If a sinusoid's frequency is so low that the same sample value is taken from the table k times, the *effective* sampling rate at that frequency has been reduced by k . Since the effective sampling rate must

¹All signal levels are relative to the mean signal level.

give two uncorrelated signals with power spectra approximating $S(f)$. The number of sinusoids is chosen to give a good approximation to the Gaussian amplitude distribution and the desired spectrum[3].

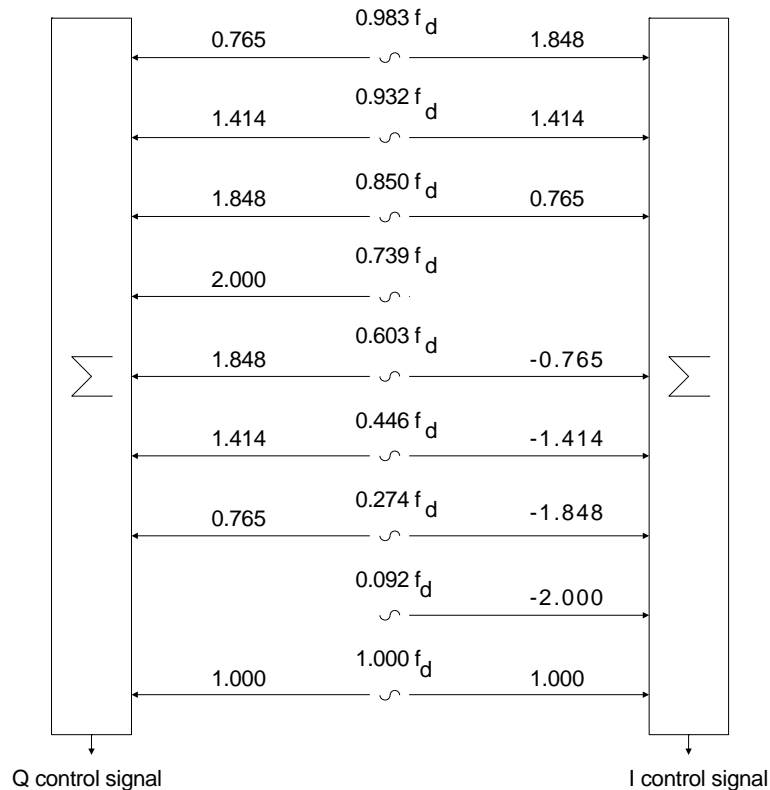


Figure B.3: Generation of the pseudo-random control signals showing the frequencies and magnitudes of the sinusoids. The frequencies of the sinusoids are shown as a fraction of the Doppler rate, f_d . The quantities along the connecting lines are the amplitudes.

A listing of the 8088 assembly-language program that generates the control signals is given in Appendix E. The program runs continuously and generates one sample every $338\mu\text{s}$. An eight-bit switch register (see Figure B.4) is read before computing the value of each sample. If the least significant bit is one (switch on), the middle six bits of the switch register give the Doppler rate in binary between 2 and 126 Hz in increments of 2 Hz. If the least significant bit is zero (switch off), the RF level is held at a fixed value.

microprocessor instead of analog components. Doppler rates between 2 and 126 Hz in steps of 2 Hz can be simulated. Figure B.2 shows how the simulator is used in a mobile radio channel simulation.

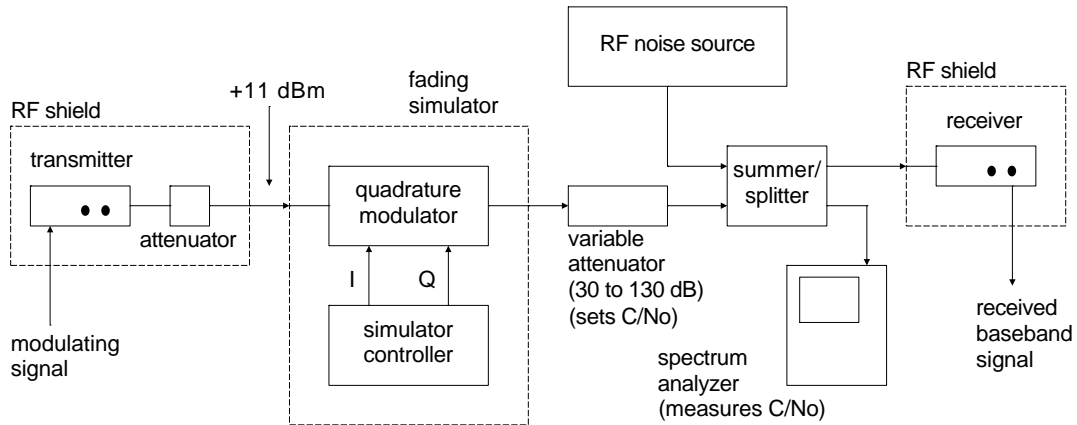


Figure B.2: Use of the simulator for mobile radio channel simulation.

The following sections describe the control section, the quadrature modulator, and how the simulator was tested.

B.2 Control Section

This section describes the unit that generates the in-phase (**I**) and quadrature (**Q**) control signals. These are independent pseudo-random Gaussian signals with low-pass power spectra proportional to

$$S(f) = \begin{cases} [1 - (f/f_d)^2]^{-\frac{1}{2}} & f \leq f_d \\ 0 & f > f_d \end{cases} \quad (\text{B.1})$$

for a (maximum) Doppler rate f_d and an omnidirectional vertical antenna[3].

B.2.1 Software Description

As shown in Figure B.3, the control signals are the weighted sums of the outputs of nine sinusoidal oscillators. The amplitudes and frequencies of the sinusoids are chosen to

Appendix B

The Fading Simulator

B.1 Introduction

A fading simulator was built to carry out the measurements described in Chapter 5. This unit simulates the multipath fading present on narrowband VHF and UHF mobile radio channels. The simulator is also described in [56].

The effects of non-frequency-selective multipath fading on a mobile radio signal can be approximated by modulating the in-phase and quadrature components of the signal with independent low-pass Gaussian random signals as shown in Figure B.1. The fading simulator consists of a quadrature modulator and a control section that generates the two random signals.

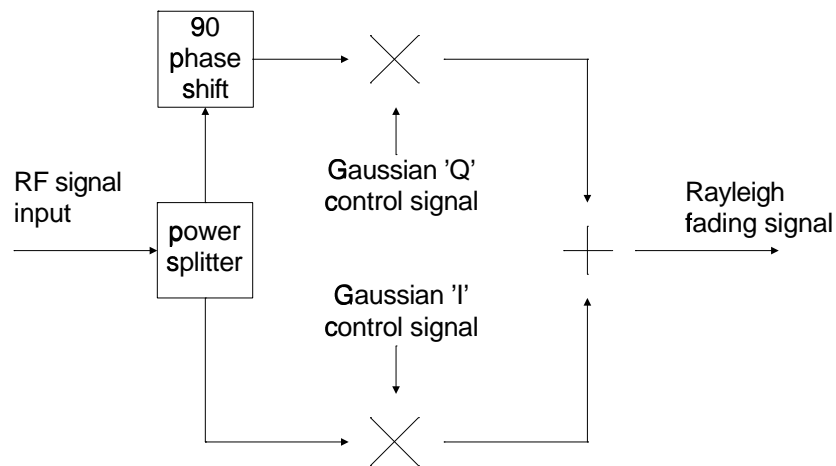


Figure B.1: Rayleigh fading is produced by modulating the in-phase and quadrature components of the RF signal with independent Gaussian random signals.

The simulator implements the method developed by Jakes [3] but uses an Intel 8088

The last term in equation A.25 can be simplified to

$$\begin{aligned}
& \frac{1}{N^2} D^2 \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} s_i s_j (W^{-2mj} - W^{2mi}) \\
&= \frac{1}{N} D^2 \left(\frac{1}{N} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} s_i s_j W^{-2mj} - \frac{1}{N} \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} s_i s_j W^{2mi} \right) \\
&= \frac{1}{N} D^2 \left(\sum_{j=0}^{N-1} s_j W^{-2mj} \frac{1}{N} \sum_{i=0}^{N-1} s_i - \sum_{i=0}^{N-1} s_i W^{2mi} \frac{1}{N} \sum_{j=0}^{N-1} s_j \right) \\
&= \frac{1}{N} D^2 \langle \mathbf{s} \rangle \left(\sum_{j=0}^{N-1} s_j W^{-2mj} - \sum_{i=0}^{N-1} s_i W^{2mi} \right). \tag{A.26}
\end{aligned}$$

As in section A.3, the sums are the DFTs of \mathbf{s} evaluated at $\pm 2m$, $S_{\pm 2m}$. Under the same conditions as in section A.3 the sums ($S_{\pm 2m}$) can be assumed to be negligible compared to $S_0 = N \langle \mathbf{s} \rangle$, so that

$$N \langle \mathbf{s} \rangle = \sum_{i=0}^{N-1} s_i \gg \sum_{i=0}^{N-1} s_i W^{\pm 2mi}. \tag{A.27}$$

Using Chebyshev's inequality [80],

$$\frac{1}{N} \sum_{i=0}^{N-1} s_i^2 \geq \langle \mathbf{s} \rangle^2, \tag{A.28}$$

and $|D|^2 = \sigma_X^2$, we find

$$\sigma_X^2 \frac{1}{N} \sum_{i=0}^{N-1} s_i^2 \geq |D|^2 \langle \mathbf{s} \rangle^2 \gg |D|^2 \frac{1}{N} \langle \mathbf{s} \rangle \sum_{i=0}^{N-1} s_i W^{\pm 2mi}. \tag{A.29}$$

Thus from A.25

$$\mathbb{E}[Y_m Y_m^*] \approx \sigma_X^2 \frac{1}{N} \sum_{i=0}^{N-1} s_i^2 + N \sigma_w^2 \frac{1}{N} \sum_{i=0}^{N-1} n_i^2, \tag{A.30}$$

and the conditional variance of the received data value is

$$\text{var}(Y_m | X_m = D, X_{-m} = D^*, \mathbf{r}) \approx \sigma_X^2 \langle \mathbf{s}^2 \rangle + N \sigma_w^2 \langle \mathbf{n}^2 \rangle - |D|^2 \langle \mathbf{s} \rangle^2. \tag{A.31}$$

So that the ratio of \mathbf{s} and \mathbf{n} corresponds to the ratio of the baseband signal and noise, the noise power, σ_w^2 , must be set equal to the baseband signal power σ_x^2 . For the case of $D = \pm 1 \pm j$, $\sigma_x^2 = 2/N$ and $\sigma_X^2 = |D|^2 = 2$, we have

$$\text{var}(Y_m | X_m = D, X_{-m} = D^*, \mathbf{r}) \approx 2 \left(\langle \mathbf{s}^2 \rangle - \langle \mathbf{s} \rangle^2 + \langle \mathbf{n}^2 \rangle \right). \tag{A.32}$$

Since the noise is zero-mean ($\mathbf{E}[w_i] = \mathbf{E}[w_j] = 0$), and \mathbf{w} and \mathbf{x} are independent,

$$\mathbf{E}[x_i w_j] = \mathbf{E}[w_i x_j] = 0 \quad (\text{A.19})$$

so that

$$\mathbf{E}[Y_m Y_m^*] = \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (s_i s_j \mathbf{E}[x_i x_j] + n_i n_j \mathbf{E}[w_i w_j]) W^{m(i-j)}. \quad (\text{A.20})$$

Using the definition of the IDFT,

$$\mathbf{E}[x_i x_j] = \frac{1}{N^2} \sum_{k=0}^{N-1} \sum_{l=0}^{N-1} \mathbf{E}[X_k X_l] W^{-ik} W^{-jl}. \quad (\text{A.21})$$

Using the conditions, and since the data symbols are zero-mean,

$$\mathbf{E}[X_k X_l] = \begin{cases} \sigma_X^2 & \text{for } k = -l \\ D^2 \delta_{km} + (D^*)^2 \delta_{k(-m)} & \text{for } k = l \\ 0 & \text{otherwise} \end{cases} \quad (\text{A.22})$$

so that

$$\begin{aligned} \mathbf{E}[x_i x_j] &= \frac{\sigma_X^2}{N^2} \sum_{k=0}^{N-1} W^{(j-i)k} + \frac{1}{N^2} D^2 W^{-im} W^{-jm} + \frac{1}{N^2} (D^*)^2 W^{im} W^{jm} \\ &= \frac{\sigma_X^2}{N} \delta_{ij} + \frac{1}{N^2} D^2 W^{-m(i+j)} - \frac{1}{N^2} D^2 W^{m(i+j)} \\ &= \frac{\sigma_X^2}{N} \delta_{ij} + \frac{1}{N^2} D^2 (W^{-m(i+j)} - W^{m(i+j)}) \end{aligned} \quad (\text{A.23})$$

since $D^2 = -(D^*)^2$ for $D = \pm 1 \pm j$.

Since \mathbf{w} is real and i.i.d. with zero mean,

$$\mathbf{E}[w_i w_j] = \sigma_w^2 \delta_{ij}. \quad (\text{A.24})$$

Substituting (A.23) and (A.24) in (A.20),

$$\begin{aligned} \mathbf{E}[Y_m Y_m^*] &= \sum_{i=0}^{N-1} \left(\frac{\sigma_X^2}{N} s_i^2 + \sigma_w^2 n_i^2 \right) W^{m(i-i)} + \\ &\quad \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} s_i s_j \frac{1}{N^2} D^2 (W^{-m(i+j)} - W^{m(i+j)}) W^{m(i-j)} \\ &= \sigma_X^2 \frac{1}{N} \sum_{i=0}^{N-1} s_i^2 + N \sigma_w^2 \frac{1}{N} \sum_{i=0}^{N-1} n_i^2 + \frac{1}{N^2} D^2 \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} s_i s_j (W^{-2mj} - W^{2mi}). \end{aligned} \quad (\text{A.25})$$

Substituting (A.9) and (A.12) in (A.8),

$$\begin{aligned} \mathbf{E}[Y_m | X_m = D, X_{-m} = D^*, \mathbf{r}] &= \sum_{n=0}^{N-1} s_n \frac{D}{N} W^{nm-nm} + \sum_{n=0}^{N-1} s_n \frac{D^*}{N} W^{nm+nm} \\ &= D \frac{1}{N} \sum_{n=0}^{N-1} s_n + D^* \frac{1}{N} \sum_{n=0}^{N-1} s_n W^{2nm}. \end{aligned} \quad (\text{A.13})$$

The term $\sum_{n=0}^{N-1} s_n W^{2nm}$ is the DFT of \mathbf{s} evaluated at a frequency of twice the sub-channel of interest (S_{2m}). If the spectrum of \mathbf{s} is concentrated below $m = 2L$ ($S_m \ll S_0$ for $|m| > 2L$) then for m between L and $\frac{N}{2} - L$ the contribution of the second term will be small so that

$$\mathbf{E}[Y_m | X_m = D, X_{-m} = D^*, \mathbf{r}] \approx D \langle \mathbf{s} \rangle. \quad (\text{A.14})$$

A.4 The Conditional Variance

The conditional variance (given the same conditions as for the mean) of a received data value Y_m , is:

$$\text{var}(Y_m | X_m = D, X_{-m} = D^*, \mathbf{r}) = \mathbf{E}[Y_m Y_m^*] - |\mathbf{E}[Y_m]|^2. \quad (\text{A.15})$$

Using the definition of the DFT, the first term can be re-written as:

$$\mathbf{E}[Y_m Y_m^*] = \mathbf{E} \left[\sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (s_i x_i + n_i w_i)(s_j x_j + n_j w_j)^* W^{mi} W^{-mj} \right]. \quad (\text{A.16})$$

Using the linearity of the expectation operator, and since \mathbf{x} , \mathbf{w} , \mathbf{s} and \mathbf{n} are real (so that $x_i^* = x_i$, $w_i^* = w_i$, etc.) this can be expanded as

$$\begin{aligned} \mathbf{E}[Y_m Y_m^*] &= \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (\mathbf{E}[s_i x_i s_j x_j] + \mathbf{E}[s_i x_i n_j w_j] \\ &\quad + \mathbf{E}[n_i w_i s_j x_j] + \mathbf{E}[n_i w_i n_j w_j]) W^{m(i-j)}. \end{aligned} \quad (\text{A.17})$$

Since \mathbf{s} and \mathbf{n} are constant because of the conditions,

$$\begin{aligned} \mathbf{E}[Y_m Y_m^*] &= \sum_{i=0}^{N-1} \sum_{j=0}^{N-1} (s_i s_j \mathbf{E}[x_i x_j] + s_i n_j \mathbf{E}[x_i w_j] \\ &\quad + n_i s_j \mathbf{E}[w_i x_j] + n_i n_j \mathbf{E}[w_i w_j]) W^{m(i-j)}. \end{aligned} \quad (\text{A.18})$$

A.3 Conditional Mean

The ensemble average of the m 'th received data value, Y_m , over the set of all possible data vectors with the m 'th data value fixed at $X_m = D$ (D is complex) and over all possible noise vectors \mathbf{w} is found conditioned on a given signal level vector \mathbf{r} (and the corresponding \mathbf{s} and \mathbf{n}). For notational convenience the conditions will often be omitted from the expected value operators although they are implied.

The received signal samples are

$$y_n = s_n x_n + n_n w_n. \quad (\text{A.6})$$

By using the definition of the DFT, the received value on the m 'th data subchannel is

$$Y_m = \sum_{n=0}^{N-1} (s_n x_n + n_n w_n) W^{mn}. \quad (\text{A.7})$$

The conditional mean of the received data values,

$$\mathbf{E}[Y_m \mid X_m = D, X_{-m} = D^*, \mathbf{r}] = \sum_{n=0}^{N-1} (\mathbf{E}[s_n x_n] + \mathbf{E}[n_n w_n]) W^{mn}. \quad (\text{A.8})$$

Since \mathbf{r} (and thus \mathbf{n}) is fixed, and the noise \mathbf{w} is zero-mean,

$$\mathbf{E}[n_n w_n] = n_n \mathbf{E}[w_n] = 0. \quad (\text{A.9})$$

Since \mathbf{s} is fixed,

$$\mathbf{E}[s_n x_n] = s_n \mathbf{E}[x_n]. \quad (\text{A.10})$$

To evaluate $\mathbf{E}[x_n]$ note that since the data values are zero-mean,

$$\mathbf{E}[X_k] = D \delta_{km} + D^* \delta_{k(-m)} \quad (\text{A.11})$$

so that

$$\mathbf{E}[x_n] = \mathbf{E} \left[\frac{1}{N} \sum_{k=0}^{N-1} X_k W^{-nk} \right] = \frac{1}{N} \sum_{k=0}^{N-1} \mathbf{E}[X_k] W^{-nk} = \frac{1}{N} [D W^{-nm} + D^* W^{nm}]. \quad (\text{A.12})$$

gain, s . The received noise samples are Gaussian random variables, w , scaled by the channel noise gain n . Both s and n are functions of the RF signal level, r , which is Rayleigh distributed. The functions $s = f_s(r)$ and $n = f_n(r)$, depend on the type of modulation and the characteristics of the receiver used.

Since the data, signal level, and noise (before fading) are generated by physically independent processes, \mathbf{x} , w and r are assumed to be statistically independent.

It will also be assumed that the spectrum of s is small above a certain frequency. Since the spectrum of r (equation B.1) lies below the Doppler rate, f_D , the spectrum of s will also be concentrated below f_D if the ‘‘S’’ portion of the SN curve is smooth so that there are few non-linearities in s to produce harmonics.

A.2.1 Data

The transmitted data vector, \mathbf{X} , is a block of N complex data values, each with energy σ_X^2 . For example, for OFDM-QAM $X_m = \pm 1 \pm j$ for all m so that $\sigma_X^2 = 2$. The N real signal samples, \mathbf{x} , which are transmitted over the channel are generated by an inverse DFT (IDFT). For the N samples to be real $X_m = X_{N-m}^*$ (or equivalently $X_m = X_{-m}^*$). This means that only $N/2$ of the complex data values are determined by the data and the remainder are their complex conjugates.

Most practical channels are bandpass channels so that frequencies at the low and high ends of the channel cannot be used. The data values for the unused channels are set to zero at the transmitter. In particular, it is assumed that X_0 and $X_{N/2}$ (both of which have only a real component) are set to zero.

A.2.2 Noise

The N real, i.i.d. (white) noise samples, w , are taken from a zero-mean Gaussian distribution having a variance σ_w^2 .

Appendix A

Conditional Mean and Variance of the Error

A.1 Notation

The notation \mathbf{a} is used to indicate a vector $\{a_0, a_1, \dots, a_{N-1}\}$.

The discrete Fourier transform (DFT) of \mathbf{a} is defined as $\mathbf{A} = \text{DFT}[\mathbf{a}]$ where

$$A_m = \sum_{n=0}^{N-1} a_n W^{mn}, \quad (\text{A.1})$$

and the inverse DFT (IDFT) of \mathbf{A} is defined as $\mathbf{a} = \text{IDFT}[\mathbf{A}]$ where

$$a_n = \frac{1}{N} \sum_{m=0}^{N-1} A_m W^{-mn}, \quad (\text{A.2})$$

and

$$W = e^{-j2\pi/N}. \quad (\text{A.3})$$

The notation $\langle a \rangle$ is used to denote the average of the vector \mathbf{a} over N samples, that is,

$$\langle a \rangle = \frac{1}{N} \sum_{i=0}^{N-1} a_i. \quad (\text{A.4})$$

The notation δ_{ij} is used for

$$\delta_{ij} = \begin{cases} 0 & \text{if } i \neq j \\ 1 & \text{if } i = j \end{cases} \quad (\text{A.5})$$

A.2 Assumptions

The received signal \mathbf{y} (see Figure 3.1) is the sum of received data and noise samples.

The received signal samples are the transmitted samples, \mathbf{x} , scaled by the channel signal

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