Verilog Links

Verilog consultants Stuart Sutherland and Cliff Cummings have published various articles that you might find useful. In particular the paper and presentation by Sutherland titled *Synthesizing SystemVerilog: Busting the Myth that SystemVerilog is only for Verification* explains some features of System Verilog that you might find useful for design.

If you don't like my Verilog style you can check out Freescale's Verilog HDL Coding standard. However, beware the warnings in the note by Cliff Cummings: [The] "Where's Waldo" Principle of Verilog Coding.