ELEX 7660 : Digital System Design
Term 201810

MIDTERM EXAMINATION - PART 2
12:30 AM – 1:20 PM
February 23, 2018

This exam has two (2) questions on four (4) pages. The marks for each question are as indicated. There are a total of 14 marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Books and notes are allowed. No electronic devices other than calculators are allowed.

This exam paper is for:

Exam 1 A00123456

Each exam is equally difficult.
Answer your own exam.

Do not start until you are told to do so.

Name: _____

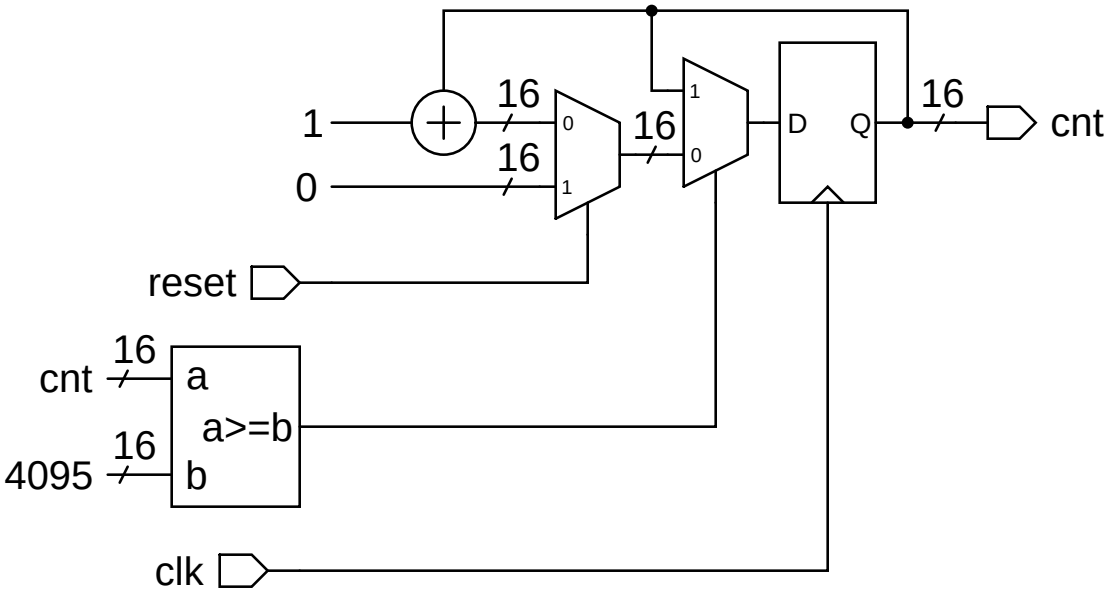
BCIT ID: _____

Signature: _____

Question	Mark	Max.
1		9
2		5
Total		16

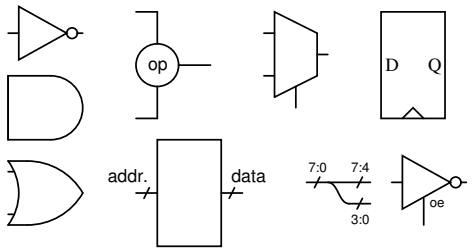
Question 1 (9 marks)

Write a System Verilog module that models the schematic shown below on the facing page. Use `logic` signal types throughout. Include all code from `module` to `endmodule`. Where the order of declarations or statements is not significant you may use any order.



Question 2 (9 marks)

Using the following symbols:



draw a schematic for the following Verilog module on the facing page. Label the inputs and outputs. Indicate the bus width if it's more than 1 bit.

```
module fract
  ( input logic [7:0] d, thr,
    output logic limit,
    input logic reset, clk ) ;

   logic [15:0] cnt, cnt_next ;

   always_comb begin
      if ( reset )
        cnt_next = '0 ;
      else
        if ( d > thr )
          cnt_next = cnt + 1 ;
        else
          cnt_next = cnt ;
   end

   always@(posedge clk)
      cnt <= cnt_next ;

   assign limit = cnt >= 16'h1000 ;

endmodule
```

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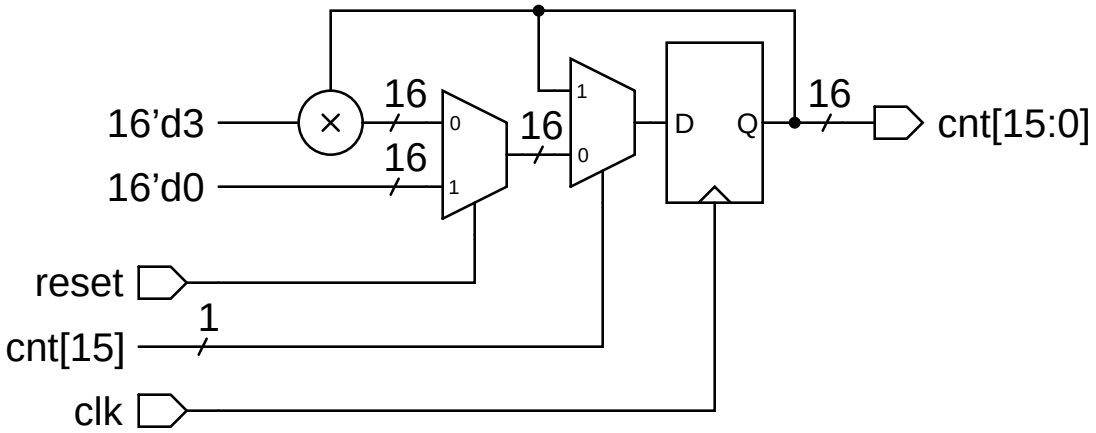
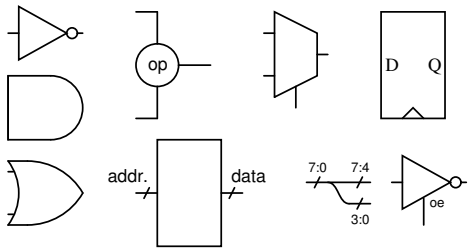


Question 2 (9 marks)

Using the following symbols:



draw a schematic for the following Verilog module on the facing page. Label the inputs and outputs. Indicate the bus width if it's more than 1 bit.

```
module accum
  ( input logic [7:0] d,
    output logic limit,
    input logic reset, clk ) ;

   logic [7:0] sum, sum_next ;

   always_comb begin
      if ( reset )
        sum_next = '0 ;
      else
        if ( d > 7'd127 && sum < 200)
          sum_next = sum + 1 ;
        else
          sum_next = sum ;
   end

   always@(posedge clk)
      sum <= sum_next ;

   assign limit = sum >= 200 ;

endmodule
```

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