4-bit binary counters 74F161A, 74F163A

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous Master Reset (74F161A)
- Synchronous Reset (74F163A)
- High speed synchronous expansion
- Typical count rate of 130MHz
- Industrial range (–40°C to +85°C) available

DESCRIPTION

4-bit binary counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock. The clock input is buffered.

The outputs of the counters may be preset to High or Low level. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D0–D3 inputs to be loaded into the counter on the positive-going edge of the clock (provided that the setup and hold requirements for $\overline{PE}$ are met). Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all the four outputs of the flip-flops (Q0 – Q3) in 74F161A to Low levels, regardless of the levels at CP, $\overline{PE}$, CET and CEP inputs (thus providing an asynchronous clear function). For the 74F163A, the clear function is synchronous. A Low level at the Synchronous Reset ($\overline{SR}$) input sets all four outputs of the flip-flops (Q0 – Q3) to Low levels after the next positive-going transition on the clock (CP) input (provided that the setup and hold time requirements for $\overline{SR}$ are met). This action occurs regardless of the levels at $\overline{PE}$, CET, and CEP inputs. The synchronous reset feature enables the designer to modify the maximum count with only one external NAND gate (see Figure 1). The carry look-ahead simplifies serial cascading of the counters. Both Count Enable (CEP and CET) inputs must be High to count. The CET input is fed forward to enable the TC output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q0. This pulse can be used to enable the next cascaded stage (see Figure 2). The TC output is subjected to decoding spikes due to internal race conditions. Therefore, it is not recommended for use as clock or asynchronous reset for flip-flops, registers, or counters.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F161A 74F163A	130MHz	46mA

ORDERING INFORMATION

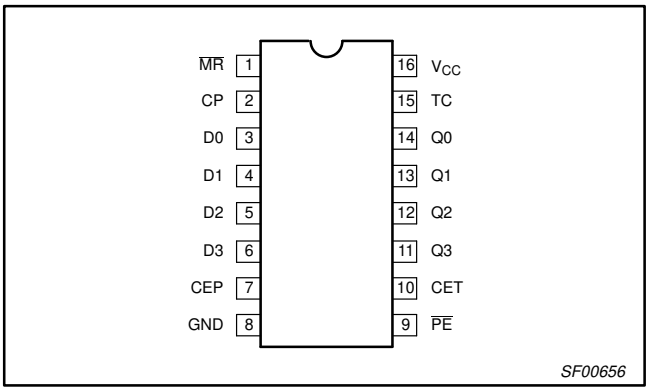
DESCRIPTION	ORDER CODE		DRAWING NUMBER
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V ±10%, T_{amb} = –40°C to +85°C	
16-pin plastic DIP	N74F161AN, N74F163AN	I74F161AN, I74F163AN	SOT38-4
16-pin plastic SO	N74F161AD, N74F163AD	I74F161AD, I74F163AD	SOT109-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

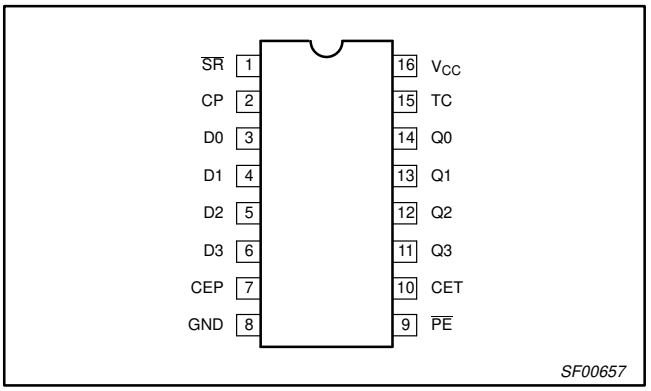
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D0 – D3	Data inputs	1.0/1.0	20µA/0.6mA
CEP	Count Enable Parallel input	1.0/1.0	20µA/0.6mA
CET	Count Enable Trickle input	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/2.0	20µA/1.2mA
$\overline{MR}$	Asynchronous Master Reset input (active Low) for 74F161A	1.0/1.0	20µA/0.6mA
$\overline{SR}$	Synchronous Reset input (active Low) for 74F163A	1.0/1.0	20µA/0.6mA
TC	Terminal count output	50/33	1.0mA/20mA
Q0 – Q3	Flip-flop outputs	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST unit load is defined as: 20µA in the High state and 0.6mA in the Low state.

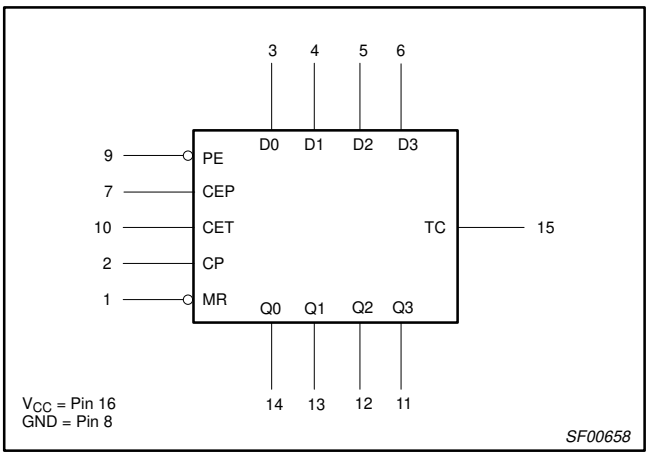
74F161A PIN CONFIGURATION



74F163A PIN CONFIGURATION



74F161A LOGIC SYMBOL



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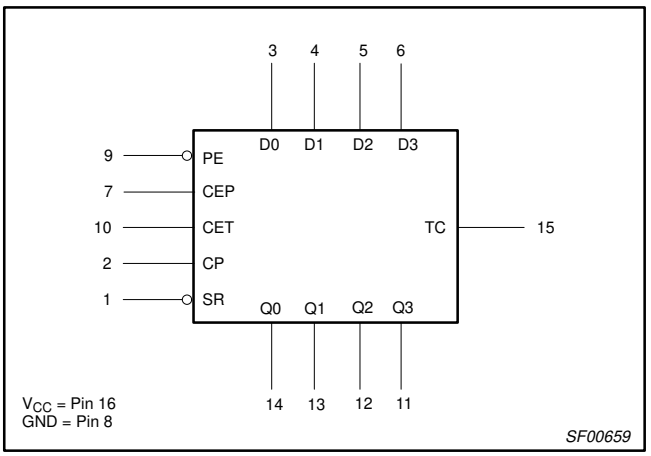
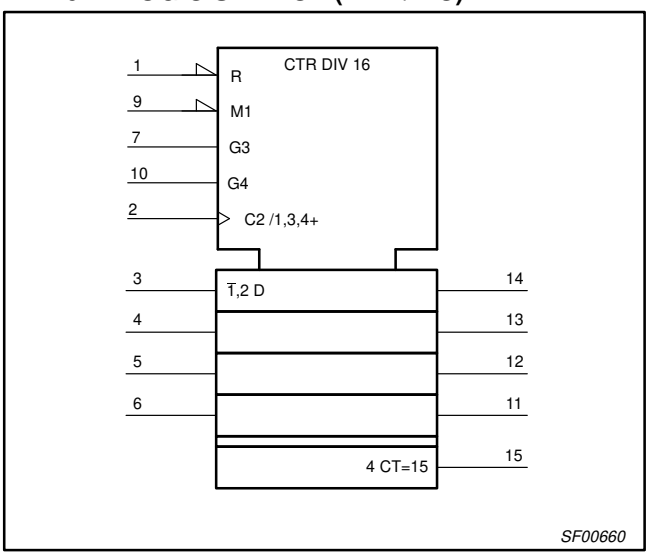
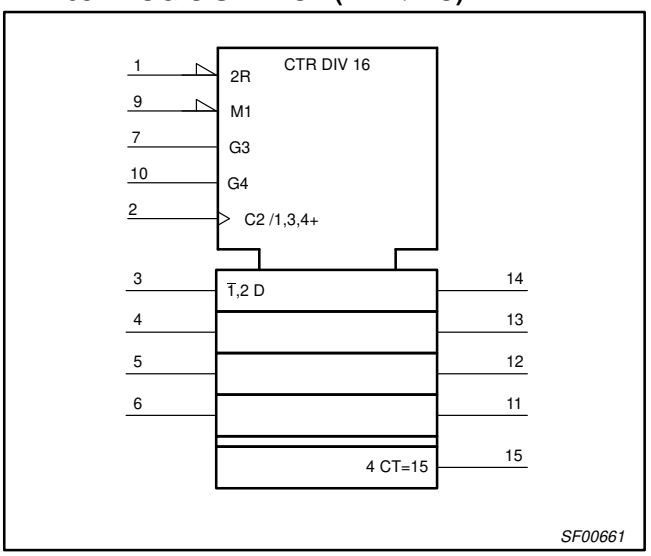


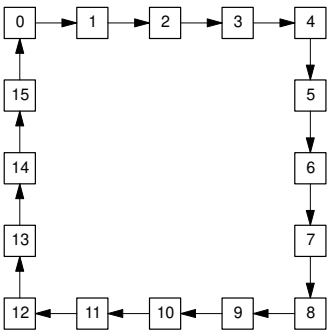
74F161A LOGIC SYMBOL (IEEE/IEC)



74F163A LOGIC SYMBOL (IEEE/IEC)



STATE DIAGRAM



LOGIC EQUATIONS:
COUNT ENABLE = CEP • CET • $\overline{PE}$
TC = Q0 • Q1 • Q2 • Q3 • CET

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APPLICATIONS

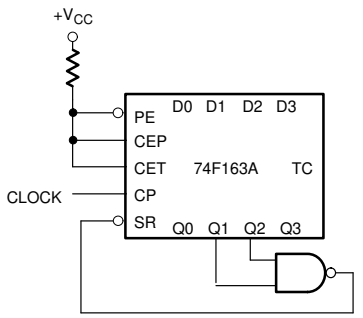

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Figure 1. Maximum count modifying scheme
Terminal count = 6

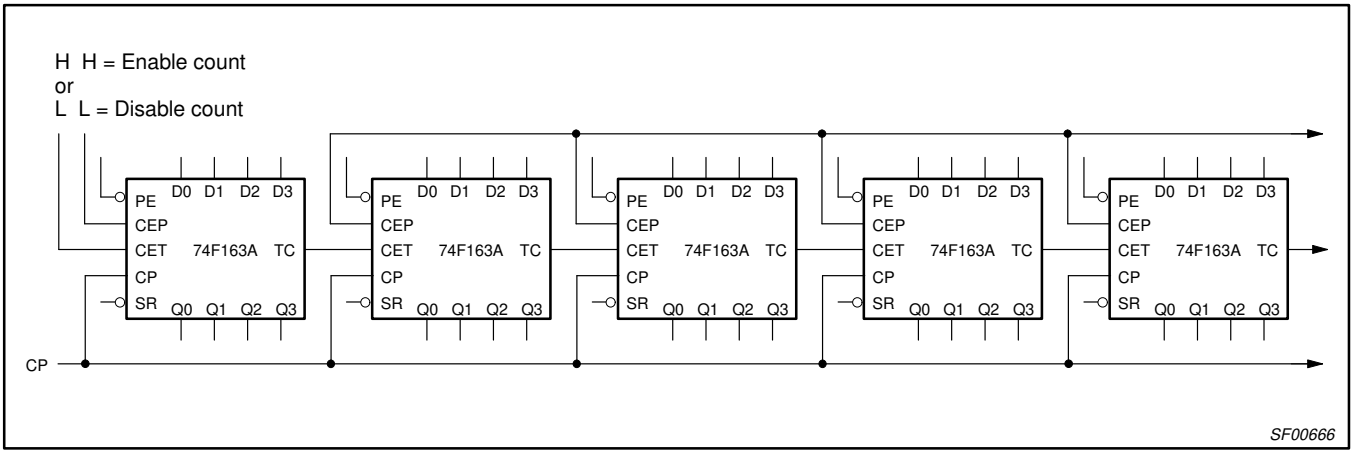

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Figure 2. Synchronous multistage counting scheme

74F161A MODE SELECT – FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	Dn	Qn	TC	
L	X	X	X	X	X	L	L	Reset (clear)
H	↑	X	X	l	l	L	L	Parallel load
H	↑	X	X	l	h	H	(1)	
H	↑	h	h	h	X	count	(1)	Count
H	X	l	X	h	X	q_n	(1)	Hold (do nothing)
H	X	X	l	h	X	q_n	L	