

**256K x 16 Bit High-Speed CMOS Static RAM(3.3V Operating)**

**FEATURES**

- Fast Access Time 10,12,15ns(Max.)
- Low Power Dissipation
  - Standby (TTL) : 50mA(Max.)
  - (CMOS) : 10mA(Max.)
  - 1.2mA(Max.)- L-Ver.
- Operating KM616V4002B/BL - 10 : 250mA(Max.)
- KM616V4002B/BL - 12 : 245mA(Max.)
- KM616V4002B/BL - 15 : 240mA(Max.)
- Single 3.3 ±0.3V Power Supply
- TTL Compatible Inputs and Outputs
- Fully Static Operation
  - No Clock or Refresh required
- Three State Outputs
- Low Data Retention Voltage : 2V(Min.) - L-Ver. Only
- Center Power/Ground Pin Configuration
- Data Byte Control :  $\overline{LB}$  : I/O<sub>1</sub>~ I/O<sub>8</sub>,  $\overline{UB}$  : I/O<sub>9</sub>~ I/O<sub>16</sub>
- Standard Pin Configuration
  - KM616V4002BJ : 44-SOJ-400
  - KM616V4002BT : 44-TSOP2-400F

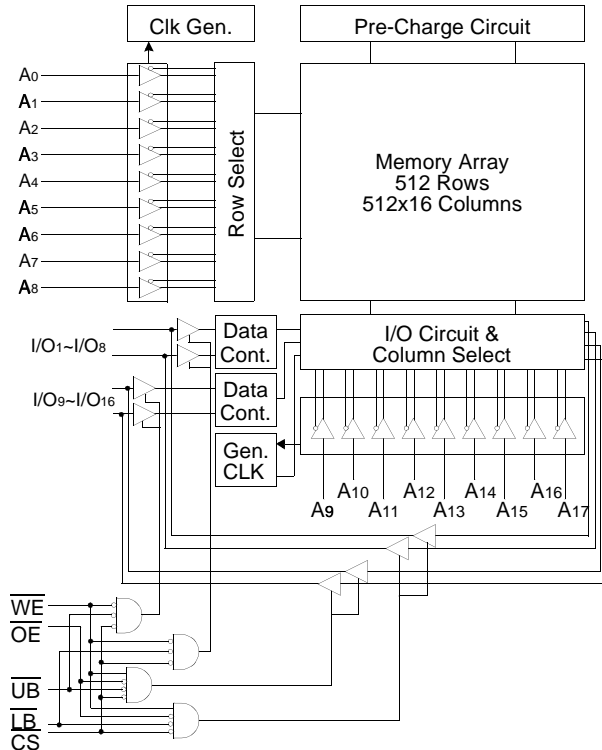
**GENERAL DESCRIPTION**

The KM616V4002B is a 4,194,304-bit high-speed Static Random Access Memory organized as 262,144 words by 16 bits. The KM616V4002B uses 16 common input and output lines and has an output enable pin which operates faster than address access time at read cycle. Also it allows that lower and upper byte access by data byte control( $\overline{UB}$ ,  $\overline{LB}$ ). The device is fabricated using SAMSUNG's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The KM616V4002B is packaged in a 400mil 44-pin plastic SOJ or TSOP(II) forward.

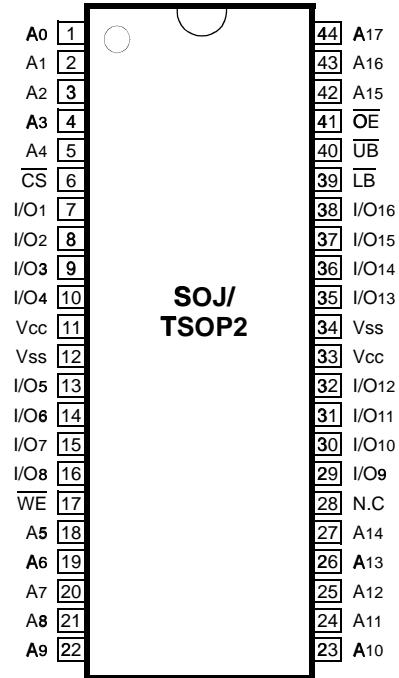
**ORDERING INFORMATION**

KM616V4002B/BL -10/12/15	Commercial Temp.
KM616V4002BI/BLI -10/12/15	Industrial Temp.

**FUNCTIONAL BLOCK DIAGRAM**



**PIN CONFIGURATION (Top View)**



**PIN FUNCTION**

Pin Name	Pin Function
A0 - A17	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{LB}$	Lower-byte Control(I/O <sub>1</sub> ~I/O <sub>8</sub> )
$\overline{UB}$	Upper-byte Control(I/O <sub>9</sub> ~I/O <sub>16</sub> )
I/O1 ~ I/O16	Data Inputs/Outputs
Vcc	Power(+3.3V)
Vss	Ground
N.C	No Connection

**ABSOLUTE MAXIMUM RATINGS\***

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to Vss		V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to 4.6	V
Voltage on Vcc Supply Relative to Vss		V <sub>CC</sub>	-0.5 to 4.6	V
Power Dissipation		P <sub>D</sub>	1.0	W
Storage Temperature		T <sub>STG</sub>	-65 to 150	°C
Operating Temperature	Commercial	T <sub>A</sub>	0 to 70	°C
	Industrial	T <sub>A</sub>	-40 to 85	°C

\* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS**(T<sub>A</sub>=0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V <sub>CC</sub>	3.0	3.3	3.6	V
Ground	V <sub>SS</sub>	0	0	0	V
Input High Voltage	V <sub>IH</sub>	2.0	-	V <sub>CC</sub> +0.3**	V
Input Low Voltage	V <sub>IL</sub>	-0.3*	-	0.8	V

NOTE: The above parameters are also guaranteed at industrial temperature range.

\* V<sub>IL</sub>(Min) = -2.0V a.c.(Pulse Width ≤ 8ns) for I ≤ 20mA

\*\* V<sub>IH</sub>(Max) = V<sub>CC</sub> + 2.0V a.c (Pulse Width ≤ 8ns) for I ≤ 20mA

**DC AND OPERATING CHARACTERISTICS**(T<sub>A</sub>=0 to 70°C, V<sub>CC</sub>=3.3±0.3V, unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit	
Input Leakage Current	I <sub>LI</sub>	V <sub>IN</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA	
Output Leakage Current	I <sub>LO</sub>	$\overline{CS}$ =V <sub>IH</sub> or $\overline{OE}$ =V <sub>IH</sub> or $\overline{WE}$ =V <sub>IL</sub> V <sub>OUT</sub> =V <sub>SS</sub> to V <sub>CC</sub>		-2	2	μA	
Operating Current	I <sub>CC</sub>	Min. Cycle, 100% Duty CS=V <sub>IL</sub> , V <sub>IN</sub> =V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OUT</sub> =0mA	Com	10ns	-	250	mA
				12ns	-	245	
			Ind.	15ns	-	240	
				10ns	-	285	
				12ns	-	270	
				15ns	-	265	
Standby Current	I <sub>SB</sub>	Min. Cycle, $\overline{CS}$ =V <sub>IH</sub>		-	50	mA	
		I <sub>SB1</sub>	f=0MHz, $\overline{CS}$ ≥V <sub>CC</sub> -0.2V, V <sub>IN</sub> ≥V <sub>CC</sub> -0.2V or V <sub>IN</sub> ≤0.2V	Normal	-		10
	L-Ver.			-	1.2		
Output Low Voltage Level	V <sub>OL</sub>	I <sub>OL</sub> =8mA		-	0.4	V	
Output High Voltage Level	V <sub>OH</sub>	I <sub>OH</sub> =-4mA		2.4	-	V	

NOTE: The above parameters are also guaranteed at industrial temperature range.

**CAPACITANCE\***(T<sub>A</sub>=25°C, f=1.0MHz)

Item	Symbol	Test Conditions	MIN	Max	Unit
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> =0V	-	8	pF
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0V	-	7	pF

\* NOTE : Capacitance is sampled and not 100% tested.

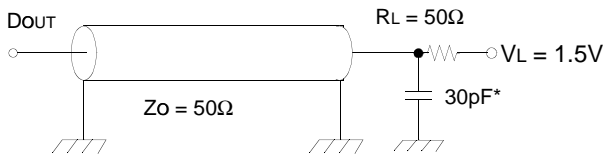
**AC CHARACTERISTICS**( $T_A=0$  to  $70^\circ\text{C}$ ,  $V_{CC}=3.3\pm 0.3\text{V}$ , unless otherwise noted.)

**TEST CONDITIONS**

Parameter	Value
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3ns
Input and Output timing Reference Levels	1.5V
Output Loads	See below

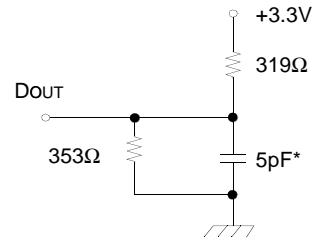
NOTE: The above test conditions are also applied at industrial temperature range.

Output Loads(A)



Output Loads(B)

for tHZ, tLZ, tWHZ, tOW, tOLZ & tOHZ



\* Capacitive Load consists of all components of the test environment.

\* Including Scope and Jig Capacitance

**READ CYCLE**

Parameter	Symbol	KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t <sub>RC</sub>	10	-	12	-	15	-	ns
Address Access Time	t <sub>AA</sub>	-	10	-	12	-	15	ns
Chip Select to Output	t <sub>CO</sub>	-	10	-	12	-	15	ns
Output Enable to Valid Output	t <sub>OE</sub>	-	5	-	6	-	7	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Access Time	t <sub>BA</sub>	-	5	-	6	-	7	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	3	-	3	-	3	-	ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	0	-	0	-	0	-	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Enable to Low-Z Output	t <sub>B LZ</sub>	0	-	0	-	0	-	ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	5	0	6	0	7	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	5	0	6	0	7	ns
$\overline{\text{UB}}$ , $\overline{\text{LB}}$ Disable to High-Z Output	t <sub>BHZ</sub>	0	5	0	6	0	7	ns
Output Hold from Address Change	t <sub>OH</sub>	3	-	3	-	3	-	ns

NOTE: The above parameters are also guaranteed at industrial temperature range.

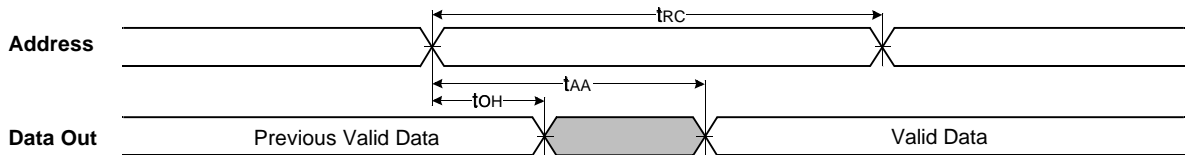
WRITE CYCLE

Parameter	Symbol	KM616V4002B/BL-10		KM616V4002B/BL-12		KM616V4002B/BL-15		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t <sub>WC</sub>	10	-	12	-	15	-	ns
Chip Select to End of Write	t <sub>CW</sub>	7	-	8	-	10	-	ns
Address Set-up Time	t <sub>AS</sub>	0	-	0	-	0	-	ns
Address Valid to End of Write	t <sub>AW</sub>	7	-	8	-	10	-	ns
Write Pulse Width( $\overline{OE}$ High)	t <sub>WP</sub>	7	-	8	-	10	-	ns
Write Pulse Width( $\overline{OE}$ Low)	t <sub>WP1</sub>	10	-	12	-	15	-	ns
$\overline{UB}$ , $\overline{LB}$ Valid to End of Write	t <sub>BW</sub>	7	-	8	-	10	-	ns
Write Recovery Time	t <sub>WR</sub>	0	-	0	-	0	-	ns
Write to Output High-Z	t <sub>WHZ</sub>	0	5	0	6	0	7	ns
Data to Write Time Overlap	t <sub>DW</sub>	5	-	6	-	7	-	ns
Data Hold from Write Time	t <sub>DH</sub>	0	-	0	-	0	-	ns
End Write to Output Low-Z	t <sub>OW</sub>	3	-	3	-	3	-	ns

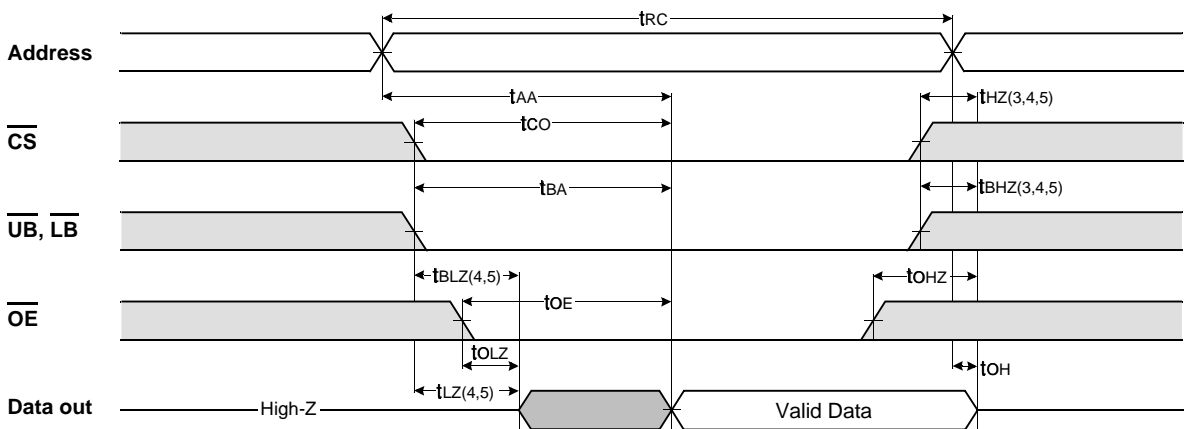
NOTE: The above parameters are also guaranteed at industrial temperature range.

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled,  $\overline{CS}=\overline{OE}=V_{IL}$ ,  $\overline{WE}=V_{IH}$ ,  $\overline{UB}$ ,  $\overline{LB}=V_{IL}$ )



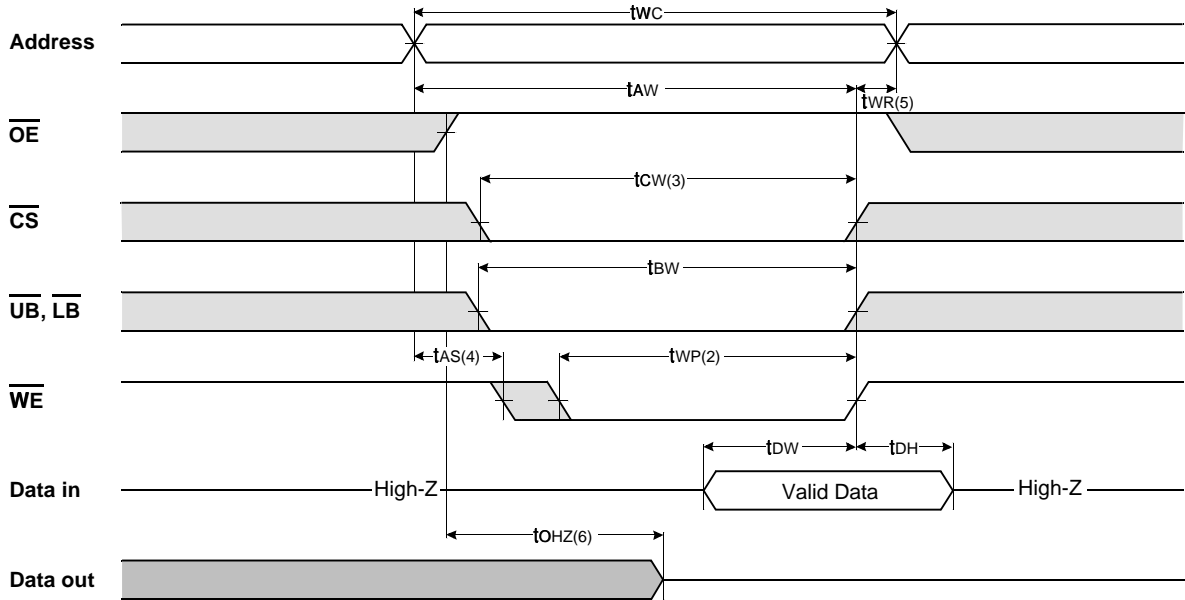
TIMING WAVEFORM OF READ CYCLE(2) ( $\overline{WE}=V_{IH}$ )



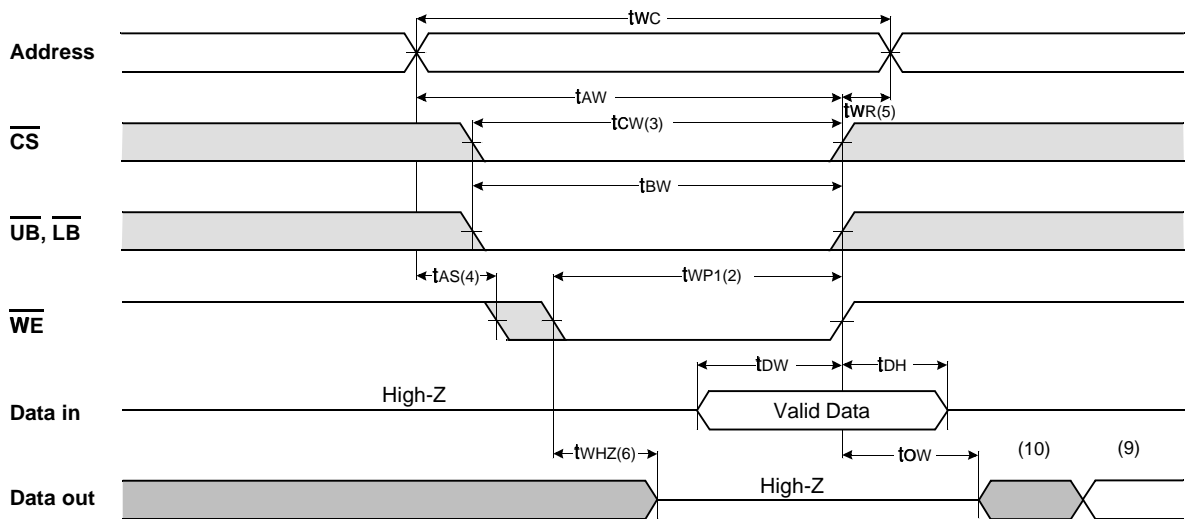
NOTES(READ CYCLE)

1.  $\overline{WE}$  is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3.  $t_{HZ}$  and  $t_{OH}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to  $V_{OH}$  or  $V_{OL}$  levels.
4. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device.
5. Transition is measured  $\pm 200\text{mV}$  from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with  $\overline{CS}=V_{IL}$ .
7. Address valid prior to coincident with  $\overline{CS}$  transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

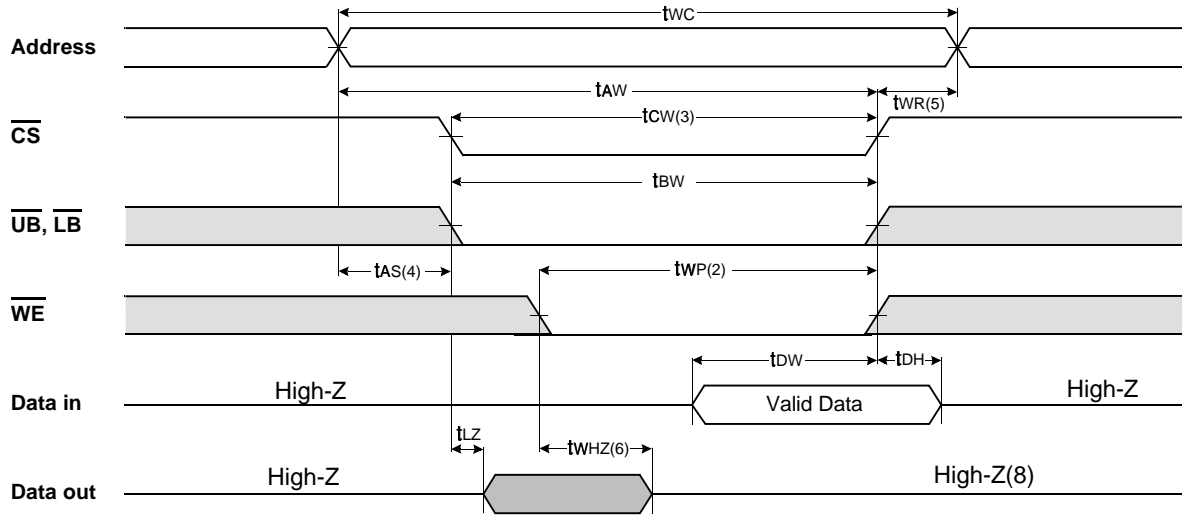
TIMING WAVEFORM OF WRITE CYCLE(1) ( $\overline{OE}$  Clock)



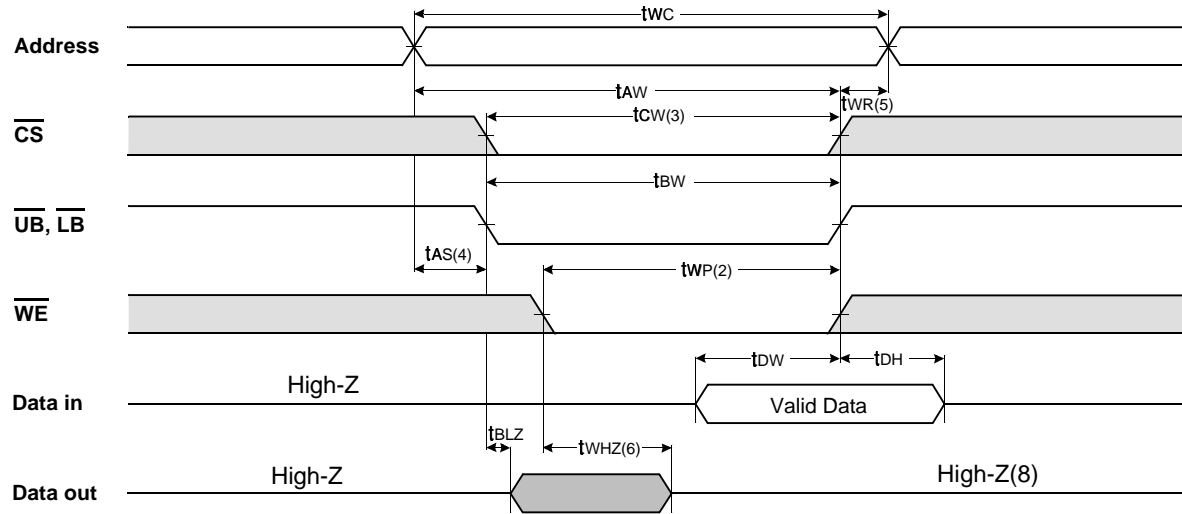
TIMING WAVEFORM OF WRITE CYCLE(2) ( $\overline{OE}$ =Low fixed)



TIMING WAVEFORM OF WRITE CYCLE(3) ( $\overline{CS}$ =Controlled)



TIMING WAVEFORM OF WRITE CYCLE(4) ( $\overline{UB}$ ,  $\overline{LB}$  Controlled)



NOTES(WRITE CYCLE)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low  $\overline{CS}$ ,  $\overline{WE}$ ,  $\overline{LB}$  and  $\overline{UB}$ . A write begins at the latest transition  $\overline{CS}$  going low and  $\overline{WE}$  going low ; A write ends at the earliest transition  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.
3.  $t_{CW}$  is measured from the later of  $\overline{CS}$  going low to end of write.
4.  $t_{AS}$  is measured from the address valid to the beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as  $\overline{CS}$  or  $\overline{WE}$  going high.
6. If  $\overline{OE}$ ,  $\overline{CS}$  and  $\overline{WE}$  are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If  $\overline{CS}$  goes low simultaneously with  $\overline{WE}$  going or after  $\overline{WE}$  going low, the outputs remain high impedance state.
9.  $D_{out}$  is the read data of the new address.
10. When  $\overline{CS}$  is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.