PIN DESCRIPTIONS

ADSP-21065L pin definitions are listed below. Inputs identified as synchronous (S) must meet timing requirements with respect to CLKIN (or with respect to TCK for TMS, TDI). Inputs identified as asynchronous (A) can be asserted asynchronously to CLKIN (or to TCK for $\overline{\text{TRST}}$).

Unused inputs should be tied or pulled to VDD or GND, except for $ADDR_{23-0}$, $DATA_{31-0}$, $FLAG_{11-0}$, $\overline{\text{SW}}$, and inputs that have internal pull-up or pull-down resistors ($\overline{\text{CPA}}$, ACK, DTxX, DRxX, TCLKx, RCLKx, TMS, and TDI)—these pins can be left floating. These pins have a logic-level hold circuit that prevents the input from floating internally.

I = Input S = Synchronous P = Power Supply (O/D) = Open Drain
O = Output A = Asynchronous G = Ground (A/D) = Active Drive
T = Three-state (when $\overline{\text{SBTS}}$ is asserted, or when the ADSP-2106x is a bus slave)

Pin	Type	Function
$ADDR_{23-0}$	I/O/T	**External Bus Address**. The ADSP-21065L outputs addresses for external memory and peripherals on these pins. In a multiprocessor system the bus master outputs addresses for read/writes of the IOP registers of the other ADSP-21065L. The ADSP-21065L inputs addresses when a host processor or multiprocessing bus master is reading or writing its IOP registers.
$DATA_{31-0}$	I/O/T	**External Bus Data**. The ADSP-21065L inputs and outputs data and instructions on these pins. The external data bus transfers 32-bit single-precision floating-point data and 32-bit fixed-point data over bits 31-0. 16-bit short word data is transferred over bits 15-0 of the bus. Pull-up resistors on unused DATA pins are not necessary.
$\overline{\text{MS}}_{3-0}$	I/O/T	**Memory Select Lines**. These lines are asserted as chip selects for the corresponding banks of external memory. Internal $ADDR_{25-24}$ are decoded into $\overline{\text{MS}}_{3-0}$. The $\overline{\text{MS}}_{3-0}$ lines are decoded memory address lines that change at the same time as the other address lines. When no external memory access is occurring the $\overline{\text{MS}}_{3-0}$ lines are inactive; they are active, however, when a conditional memory access instruction is executed, whether or not the condition is true. Additionally, an $\overline{\text{MS}}_{3-0}$ line which is mapped to SDRAM may be asserted even when no SDRAM access is active. In a multiprocessor system, the $\overline{\text{MS}}_{3-0}$ lines are output by the bus master.
$\overline{\text{RD}}$	I/O/T	**Memory Read Strobe**. This pin is asserted when the ADSP-21065L reads from external memory devices or from the IOP register of another ADSP-21065L. External devices (including another ADSP-21065L) must assert $\overline{\text{RD}}$ to read from the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{RD}}$ is output by the bus master and is input by another ADSP-21065L.
$\overline{\text{WR}}$	I/O/T	**Memory Write Strobe.** This pin is asserted when the ADSP-21065L writes to external memory devices or to the IOP register of another ADSP-21065L. External devices must assert $\overline{\text{WR}}$ to write to the ADSP-21065L's IOP registers. In a multiprocessor system, $\overline{\text{WR}}$ is output by the bus master and is input by the other ADSP-21065L.
$\overline{\text{SW}}$	I/O/T	**Synchronous Write Select.** This signal interfaces the ADSP-21065L to synchronous memory devices (including another ADSP-21065L). The ADSP-21065L asserts $\overline{\text{SW}}$ to provide an early indication of an impending write cycle, which can be aborted if $\overline{\text{WR}}$ is not later asserted (e.g., in a conditional write instruction). In a multiprocessor system, $\overline{\text{SW}}$ is output by the bus master and is input by the other ADSP-21065L to determine if the multiprocessor access is a read or write. $\overline{\text{SW}}$ is asserted at the same time as the address output.
ACK	I/O/S	**Memory Acknowledge**. External devices can deassert ACK to add wait states to an external memory access. ACK is used by I/O devices, memory controllers, or other peripherals to hold off completion of an external memory access. The ADSP-21065L deasserts ACK as an output to add wait states to a synchronous access of its IOP registers. In a multiprocessor system, a slave ADSP-21065L deasserts the bus master's ACK input to add wait state(s) to an access of its IOP registers. The bus master has a keeper latch on its ACK pin that maintains the input at the level to which it was last driven.
$\overline{\text{SBTS}}$	I/S	**Suspend Bus Three-State.** External devices can assert $\overline{\text{SBTS}}$ to place the external bus address, data, selects, and strobes—but not SDRAM control pins—in a high impedance state for the following cycle. If the ADSP-21065L attempts to access external memory while $\overline{\text{SBTS}}$ is asserted, the processor will halt and the memory access will not finish until $\overline{\text{SBTS}}$ is deasserted. $\overline{\text{SBTS}}$ should only be used to recover from host processor/ADSP-21065L deadlock.
$\overline{\text{IRQ}}_{2-0}$	I/A	Interrupt Request Lines. May be either edge-triggered or level-sensitive.
$FLAG_{11-0}$	I/O/A	Flag Pins. Each is configured via control bits as either an input or an output. As an input, it can be tested as a condition. As an output, it can be used to signal external peripherals.

POWER DISSIPATION ADSP-21065L

These specifications apply to the internal power portion of V_{DD} only. See the Power Dissipation section of this data sheet for calculation of external supply current and total supply current. For a complete discussion of the code used to measure power dissipation, see the technical note SHARC Power Dissipation Measurements.

Specifications are based on the following operating scenarios:

Table II. Internal Current Measurements

Operation	Peak Activity ($I_{DDINPEAK}$)	High Activity ($I_{DDINHIGH}$)	Low Activity ($I_{DDINLOW}$)
Instruction Type	Multifunction	Multifunction	Single Function
Instruction Fetch	Cache	Internal Memory	Internal Memory
Core Memory Access	2 per Cycle (DM and PM)	1 per Cycle (DM)	None
Internal Memory DMA	1 per Cycle	1 per 2 Cycles	1 per 2 Cycles

To estimate power consumption for a specific application, use the following equation where % is the amount of time your program spends in that state:

$$\%PEAK \times I_{DDINPEAK} + \%HIGH \times I_{DDINHIGH} + \%LOW \times I_{DDINLOW} + \%IDLE16 \times I_{DDIDLE16} = POWER\ CONSUMPTION$$

Table III. Internal Current Measurement Scenarios

Parameter		Test Conditions	Max	Units
$I_{DDINPEAK}$	Supply Current (Internal)[1]	t_{CK} = 33 ns, V_{DD} = max	470	mA
		t_{CK} = 30 ns, V_{DD} = max	510	mA
$I_{DDINHIGH}$	Supply Current (Internal)[2]	t_{CK} = 33 ns, V_{DD} = max	275	mA
		t_{CK} = 30 ns, V_{DD} = max	300	mA
$I_{DDINLOW}$	Supply Current (Internal)[3]	t_{CK} = 33 ns, V_{DD} = max	240	mA
		t_{CK} = 30 ns, V_{DD} = max	260	mA
I_{DDIDLE}	Supply Current (IDLE)[4]	t_{CK} = 33 ns, V_{DD} = max	105	mA
		t_{CK} = 30 ns, V_{DD} = max	110	mA
$I_{DDIDLE16}$	Supply Current (IDLE16)[5]	V_{DD} = max	20	mA

NOTES
[1]The test program used to measure $I_{DDINPEAK}$ represents worst case processor operation and is not sustainable under normal application conditions. Actual internal power measurements made using typical applications are less than specified.
[2]$I_{DDINHIGH}$ is a composite average based on a range of high activity code.
[3]$I_{DDINLOW}$ is a composite average based on a range of low activity code.
[4]IDLE denotes ADSP-21065L state during execution of IDLE instruction.
[5]IDLE16 denotes ADSP-21065L state during execution of IDLE16 instruction.

TIMING SPECIFICATIONS

General Notes

Two speed grades of the ADSP-21065L are offered, 60 MHz and 66 MHz instruction rates. The specifications shown are based on a CLKIN frequency of 30 MHz (t_{CK} = 33.3 ns). The DT derating allows specifications at other CLKIN frequencies (within the min–max range of the t_{CK} specification; see Clock Input below). DT is the difference between the actual CLKIN period and a CLKIN period of 33.3 ns:

$$DT = (t_{CK} - 33.3)/32$$

Use the exact timing information given. Do not attempt to derive parameters from the addition or subtraction of others. While addition or subtraction would yield meaningful results for an individual device, the values given in this data sheet reflect statistical variations and worst cases. Consequently, you cannot meaningfully add parameters to derive longer times.

See Figure 27 in Equivalent Device Loading for AC Measurements (Includes All Fixtures) for voltage reference levels.

Memory Read—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Units
Timing Requirements:				
t_{DAD}	Address, Selects Delay to Data Valid[1, 2]		28.0 + 32 DT + W	ns
t_{DRLD}	$\overline{RD}$ Low to Data Valid[1]		24.0 + 26 DT + W	ns
t_{HDA}	Data Hold from Address Selects[3]	0.0		ns
t_{HDRH}	Data Hold from $\overline{RD}$ High[3]	0.0		ns
t_{DAAK}	ACK Delay from Address, Selects[2, 3]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{RD}$ Low[3]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DRHA}	Address, Selects Hold After $\overline{RD}$ High	–1.0 + H		ns
t_{DARL}	Address, Selects to $\overline{RD}$ Low[2]	3.0 + 6 DT		ns
t_{RW}	$\overline{RD}$ Pulsewidth	25.0 + 26 DT + W		ns
t_{RWR}	$\overline{RD}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 6 DT + HI		ns
t_{RDGL}	$\overline{RD}$ High to $\overline{DMAG}$x Low	11.0 +12 DT + HI		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
HI = t_{CK} (if an address hold cycle or bus idle cycle occurs, as specified in WAIT register; otherwise HI = 0).
H = t_{CK} (if an address hold cycle occurs as specified in WAIT register; otherwise H = 0).

NOTES
[1]Data Delay/Setup: User must meet t_{DAD} or to t_{DRLD} or synchronous specification t_{SSDATI}.
[2]The falling edge of $\overline{MSx}$, $\overline{SW}$, $\overline{BMS}$, are referenced.
[3]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).

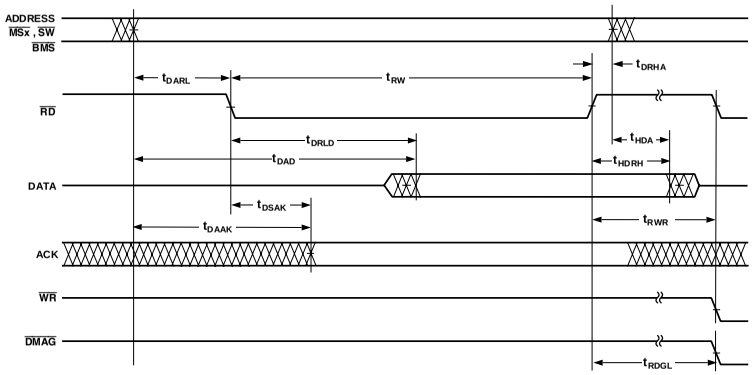

Figure 11. Memory Read—Bus Master

Memory Write—Bus Master

Use these specifications for asynchronous interfacing to memories (and memory-mapped peripherals) without reference to CLKIN. These specifications apply when the ADSP-21065L is the bus master when accessing external memory space. These switching characteristics also apply for bus master synchronous read/write timing (see Synchronous Read/Write—Bus Master below). If these timing requirements are met, the synchronous read/write timing can be ignored (and vice versa). An exception to this is the ACK pin timing requirements as described in the note below.

Parameter		Min	Max	Units
Timing Requirements:				
t_{DAAK}	ACK Delay from Address[1, 2]		24.0 + 30 DT + W	ns
t_{DSAK}	ACK Delay from $\overline{WR}$ Low[1]		19.5 + 24 DT + W	ns
Switching Characteristics:				
t_{DAWH}	Address, Selects to $\overline{WR}$ Deasserted[2]	29.0 + 31 DT + W		ns
t_{DAWL}	Address, Selects to $\overline{WR}$ Low[2]	3.5 + 6 DT		ns
t_{WW}	$\overline{WR}$ Pulsewidth	24.5 + 25 DT + W		ns
t_{DDWH}	Data Setup Before $\overline{WR}$ High	15.5 + 19 DT + W		ns
t_{DWHA}	Address Hold After $\overline{WR}$ Deasserted	0.0 + 1 DT + H		ns
t_{DATRWH}	Data Disable After $\overline{WR}$ Deasserted[3]	1.0 + 1 DT + H	4.0 + 1 DT + H	ns
t_{WWR}	$\overline{WR}$ High to $\overline{WR}$, $\overline{RD}$ Low	4.5 + 7 DT + H		ns
t_{WRDGL}	$\overline{WR}$ High to $\overline{DMAG}$x Low	11.0 + 13 DT + H		ns
t_{DDWR}	Data Disable Before $\overline{WR}$ or $\overline{RD}$ Low	3.5 + 6 DT + I		ns
t_{WDE}	$\overline{WR}$ Low to Data Enabled	4.5 + 6 DT		ns

W = (number of wait states specified in WAIT register) × t_{CK}.
H = t_{CK} (if an address hold cycle occurs, as specified in WAIT register; otherwise H = 0).
I = t_{CK} (if a bus idle cycle occurs, as specified in WAIT register; otherwise I = 0).

NOTES
[1]ACK is not sampled on external memory accesses that use the *Internal* wait state mode. For the first CLKIN cycle of a new external memory access, ACK must be valid by t_{DAAK} or t_{DSAK} or synchronous specification t_{SACKC} for wait state modes *External*, *Either*, or *Both* (*Both*, if the internal wait state is zero). For the second and subsequent cycles of a wait stated external memory access, synchronous specifications t_{SACKC} and t_{HACKC} must be met for wait state modes *External*, *Either*, or *Both* (*Both*, after internal wait states have completed).
[2]The falling edge of $\overline{MSx}$, $\overline{SW}$, and $\overline{BMS}$ is referenced.
[3]See System Hold Time Calculation under Test Conditions for calculation of hold times given capacitive and dc loads.

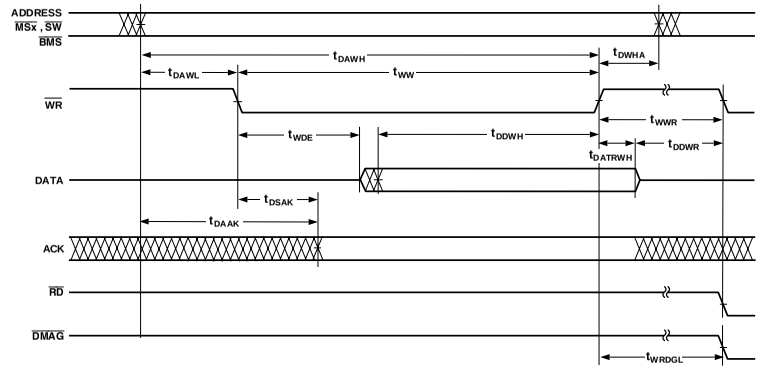

Figure 12. Memory Write—Bus Master