ELEX 2117 : Digital Techniques 2
2021 Winter Term

Combinational Logic Design with Verilog

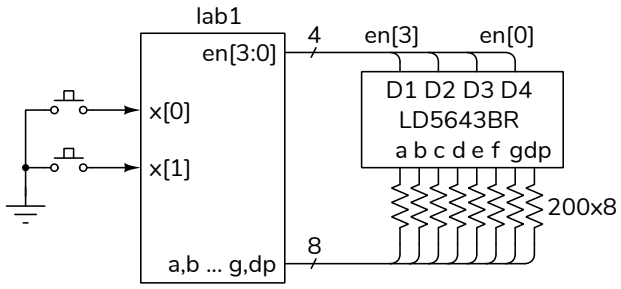
Introduction

This lab introduces logic synthesis using Verilog. You will need the following from your ELEX 1117 and 2117 parts kits:

- solderless breadboard
- EPM240T100C5 CPLD board, Byte Blaster JTAG interface and coaxial power connector,
- an LD5643BR 4-digit 7-segment LED display[1]
- $7 \times 200\ \Omega$ resistors
- two SPST N.O. pushbutton switches
- pin-header jumpers

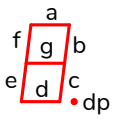
Circuit Description

The following block diagram shows how the pushbutton switches and LED are connected to the CPLD:



The two pushbuttons, **x[0]** and **x[1]**, are the active-low inputs to your design. These inputs will be configured with internal pull-up resistors.

The display contains four 7-segment displays. The active-high digit-enable outputs are **en[3]** through **en[0]** in order form left to right and the active-low segment-enable outputs are **a** through **g**:



[1]Note that Lee's Electronics links to the wrong datasheet.

Active-low means an input or output is at a low logic level when it's true. We will consider a switch to be "true" when pressed and an LED digit or segment is "true" when lit.

Your circuit should display the last four digits of *your* BCIT ID in the appropriate digit position when the switch inputs, treated as a binary number, have values of 0 through 3. For example, if you BCIT ID is A00123456 then when both switches are false (not pressed) the LED should show 3 on the leftmost digit and when the rightmost switch is pressed (**x[0]** is low) then the LED should show 4 in the second digit, etc. The truth table defining the input-to-output relationship for an ID of A00123456 is:

x[1]	x[0]	en[3:0]	LED
0	0	1000	3
0	1	0100	4
1	0	0010	5
1	1	0001	6

Note that the table above shows the *logical* values of **x**. This means that a **1** indicates "true" which corresponds to a *low* logic level for **x[*i*]** and a *high* level for **en[*i*]**. Verilog uses the values 0 and 1 for low and high logic levels respectively when specifying input and output values. But it also uses 0 and 1 for arithmetic and truth values. This can be confusing so you need to pay attention to the context.

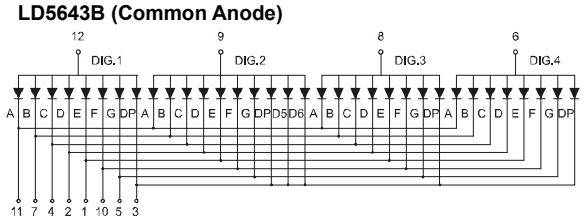
CPLD and LED Interfaces

The tables and photos below show one way to connect the CPLD to the switches and the LED. You may use different pins; for example, if some of your IO pins are damaged.

You will configure internal pull-up resistors on **x[0]** and **x[1]** so that the N.O. (normally open) pushbutton switch contacts produce a low logic level when pressed.

Your ELEX 2117 parts kit contains an LD5643BR (or compatible) display. The multiplexed common-anode configuration has one anode per digit but the

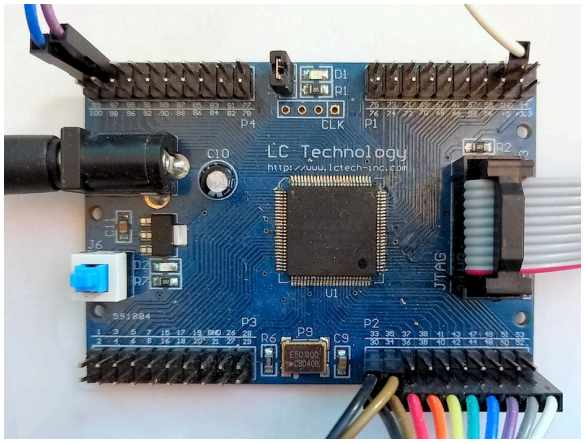
cathodes for each segment are connected together as you can see from the schematic: [2]

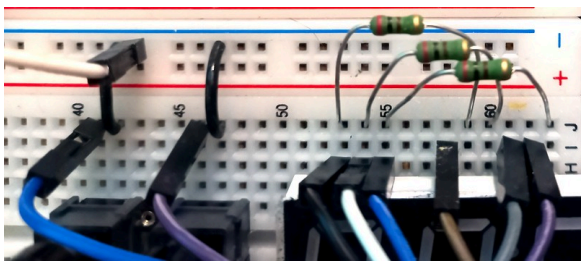


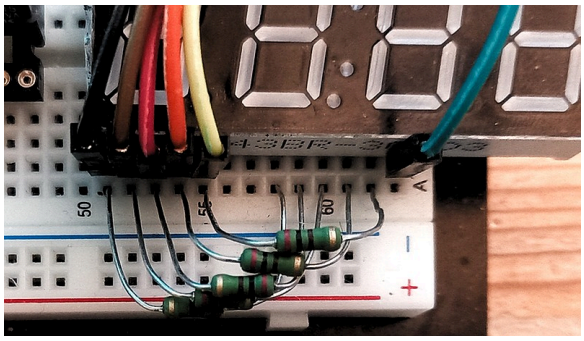
To display a number in a particular digit position your circuit must set the appropriate anode to a high voltage and set the cathodes of the segments that are to be lit to a low voltage.

Since the LED package only has 12 pins, the colon (D5, D6) and decimal point (dp)have been connected together internally[3]. You can force this pin high (1) to turn it off or connect it to one of the signals in your design when troubleshooting.

The following photos and tables show how the LED segments are connected to the CPLD pins on connectors P2 and P4 of the CPLD board:



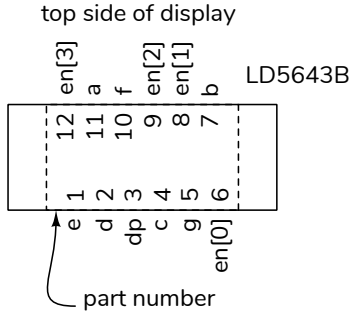




LED Pin	wire colour	segment	CPLD pin
1	black	e	30
2	brown	d	34
3	red	dp	36
4	orange	c	38
5	yellow	g	40
6	green	en[0]	42
7	blue	b	44
8	violet	en[1]	48
9	gray	en[2]	50
10	white	f	52
11	black	a	33
12	brown	en[3]	35

wire color	CPLD pin	switch
blue (7)	99	x[1]
violet (6)	97	x[0]

Note the use of colour coding and that you may have different pushbutton switches in your parts kits. The switch for x[1] is mounted on the left. For reference, the display pinout is:



Procedure

Follow the general procedure in the Software Installation and Use document on the course web site to

[2]Diagram from LD5463 datasheet.

[3]On my display the decimal points (DP) are not connected.

create a project, compile it and configure your CPLD. Connect the CPLD board to the switches and LED. Test your design and fix any errors.

Internal Pull-Up Resistors

When you assign signals to pins you'll also need to configure internal pull-up resistors on the two input pins. Open the Assignment Editor (**Assignments > Assignment Editor**). Double-click on «new». in the **To** column and enter the pin name (`x[0]`). Select **Weak Pull-Up Resistor** from the drop-down menu in the **Assignment Name** column. Select **On** from the drop-down menu in the **Value** column. Repeat for `x[1]`.

If you used the pin assignments above you should end up with the following:

	To	Assignment Name	Value
out	a	Location	PIN_33
out	b	Location	PIN_44
out	c	Location	PIN_38
out	d	Location	PIN_34
out	dp	Location	PIN_36
out	e	Location	PIN_30
out	en[3]	Location	PIN_35
out	en[2]	Location	PIN_50
out	en[1]	Location	PIN_48
out	en[0]	Location	PIN_42
out	f	Location	PIN_52
out	g	Location	PIN_40
in	x[1]	Location	PIN_99
in	x[0]	Location	PIN_97
in	x[0]	Weak Pull-Up Resistor	On
in	x[1]	Weak Pull-Up Resistor	On

Hints

1. You can use the Verilog concatenation operator (`{,}`) in both the left- and right-hand sides of an assignment. For example:

```
...
   assign {en,a,b,c,d,e,f,g}
     = x == 2'b11 ? {4'b1000,7'h06} :
...
```

2. To save you time, here are the active-low seven-segment values (`a` to `g`) for digits 0 to 9:

```
0  7'h01
1  7'h4f
2  7'h12
3  7'h06
4  7'h4c
5  7'h24
6  7'h20
7  7'h0f
8  7'h00
9  7'h04
```

3. We'll be using the same display in later labs. Leave the LED connected if you have enough space on your breadboard.

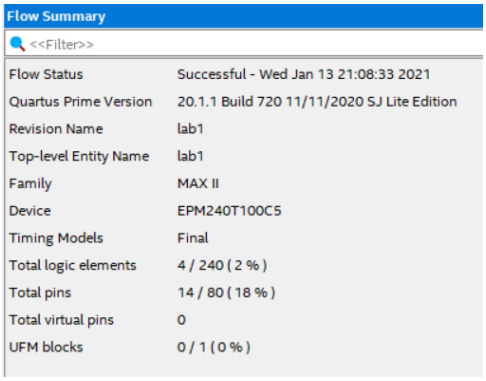
4. You may want to use ModelSim to check your code for syntax errors – it compiles much faster.

Submissions

Submit the following to the appropriate Assignment folder on the course website:

1. A PDF document containing:

   - A listing of your Verilog code.
   - A screen capture of your compilation report, for example:



2. A video showing the pushbuttons and the LED display as you test the four pushbutton states in the order shown above (`2'b00` to `2'b11` corresponding to the leftmost to rightmost digit). The LED should, of course, show the last four digits of *your* BCIT ID.