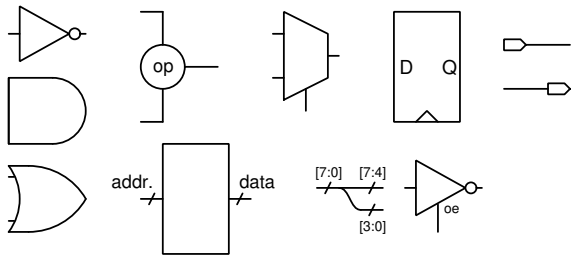
Solutions to Practice Quiz 2

Question 1:

Using the following schematic symbols:

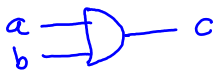


and these declarations:

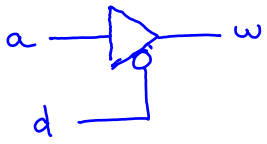
```
type byte_array is array (natural range <>) of
  std_logic_vector(7 downto 0) ;
signal a, b, c, d, w, clk : std_logic ;
signal x, y, z, y_next, n : unsigned (7 downto 0) ;
signal r, s : unsigned (31 downto 0) ;
signal m : byte_array (0 to 3) ;
signal p : unsigned(1 downto 0) ;
```

convert each of the following VHDL expressions into a schematic:

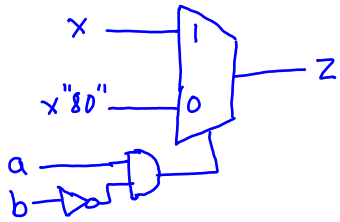
(a) `a <= b or c ;`



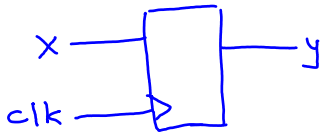
(b) `w <= a when d = '0' else 'Z' ;`



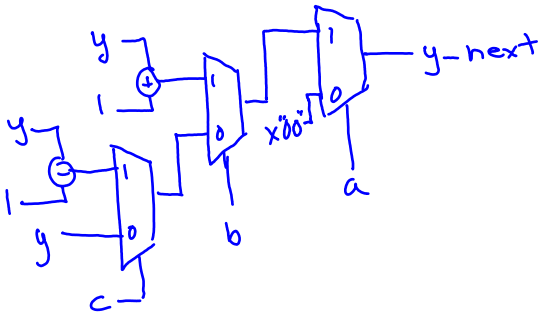
(c) `z <= x when a = '1' and b = '0' else x"80" ;`

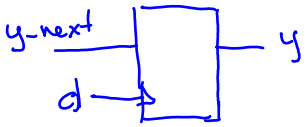


(d) `y <= x when rising_edge(clk) ;`

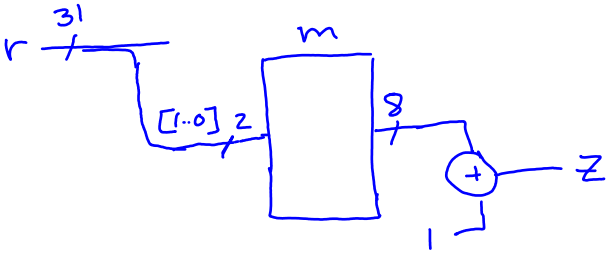


(e)
```
y_next <= x"00" when a = '0' else
          y+1 when b = '1' else
          y-1 when c = '1' else
          y ;
y <= y_next when rising_edge(d) ;
```





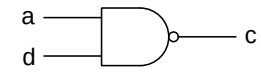
(f) `z <= unsigned(m(to_integer(r(1 downto 0))))+1 ;`



Question 2:

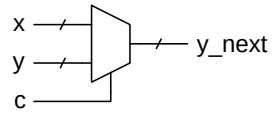
Assuming the above signal declarations and schematic symbols, write concurrent VHDL statements that would result in the following schematics:

(a)



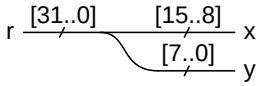

```
c <= not (a and b);
```

(b)



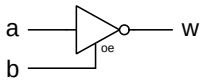

```
y_next <= x when c='1'
          else y;
```

(c)



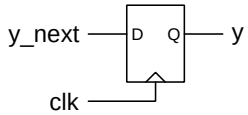

```
x <= r(15 downto 8);
y <= r(7 downto 0);
```

(d)



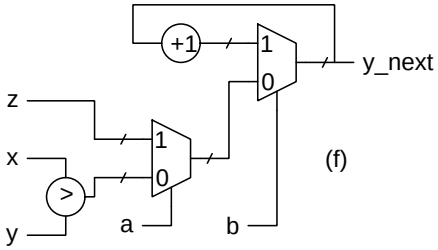

```
w <= not a when b='1'
     else 'Z';
```

(e)



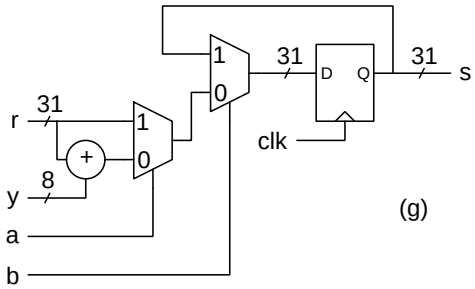

```
y <= y_next when rising_edge(clk);
```

(f)




```
y_next <= y_next + 1 when b='1'
          else z when a='1'
          else x > y; -- ???
```

(g)




```
s <= s_next when rising_edge(clk);
s_next <= s when b = '1' else
          r when a = '1' else
          r + y;
```