ELEX 2117 : Digital Techniques 2
2020 Winter Term

Quiz 1

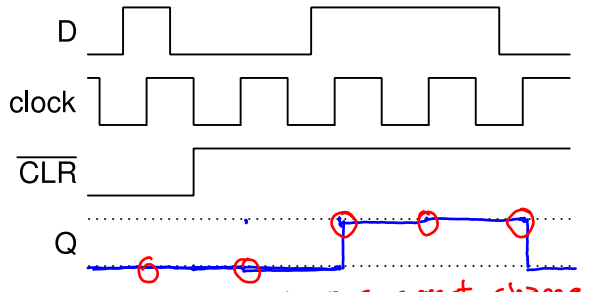
This exam is for the student whose...

surname begins with	BCIT ID ends with

Question	1	2	3	4	Total
Mark					
Out of	13	14	2	8	37

Question 1: flip-flops

Fill in the missing waveform below. Signals with an overbar are active-low. $\overline{\text{CLR}}$ is an asynchronous reset.



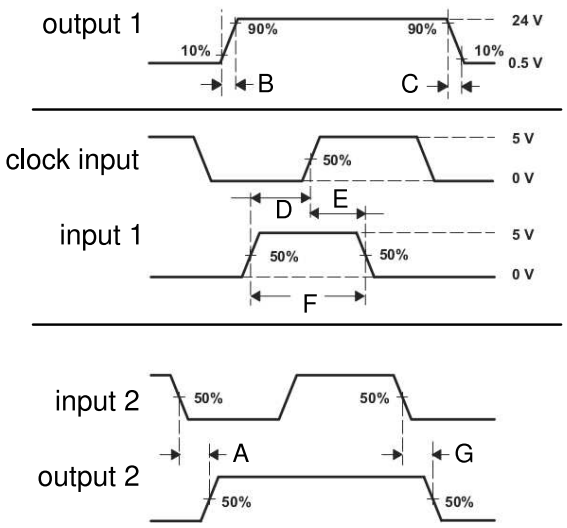
1 mark per correct change

Fill in the missing portions of the following truth tables. Use ↑ for a rising edge, Q_0 for the previous output, and × for "don't care" (meaning this input has no effect).

J	K	$\overline{\text{CLR}}$	clk	Q	$\overline{Q}$
1	1	0	↑	0	1
0	1	1	↑	0	1
1	0	1	↑	1	0
1	1	1	↑	$\overline{Q_0}$	Q_0

1 mark per correct entry (8)

Question 2: timing specifications



Fill in the following table based on the timing diagram above. For each specification labelled above, give the name of the timing specification (e.g. rise time), the common **var**iable name (e.g. t_{SU}). In the "R/G" column place a "G" if the specification is a guaranteed response or "R" if the specification is a timing requirement.
A "requirement" (R) means the circuit design must ensure this specification is met to ensure correct operation of the device. A "guaranteed response" (G) means the manufacturer guarantees this specification if the device is operated within requirements.

letter	name	var.	R/G
A	propagation delay	t_{PD}	G
B	rise time	t_R	G
C	fall time	t_F	G
D	setup time	t_{SU}	R
E	hold time	t_H	R
F	pulse width	—	R
G	propagation delay	t_{PD}	G

7 mark — 7 marks (if either correct)

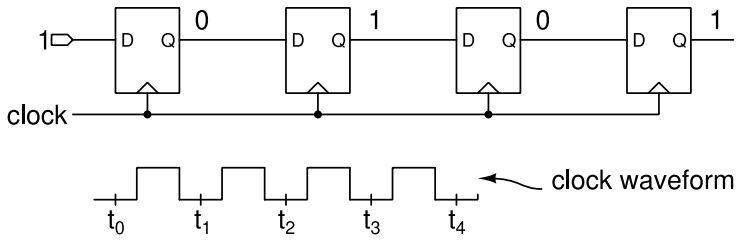
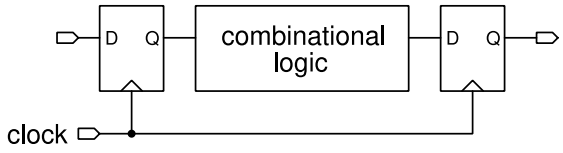


Figure 1: Shift register.

Question 3: timing calculations

In the diagram below, both flip-flops have a t_{CO} of 5 ns and a t_{SU} of 3 ns. The propagation delay through the combinational logic is 12 ns.



What is maximum clock frequency at which this circuit will operate properly?

$T_{clock\ (min)} = T_{CO} + T_{PD} + T_{SU}$

$= 5 + 12 + 3 = 20\,ns$

$f_{max} = \frac{1}{T_{(min)}} = \frac{1}{20 \times 10^{-9}} = 50\,MHz$

marks { 1 for adding up the right things
1 for correct answer

Question 4: registers

Figure 65 shows four registers and a clock waveform. The contents of the registers at time t_0 are shown at the register outputs. The value at the input to the left-most register is fixed at the value shown.
What are the contents of the four registers at time t_2?

time	input	Q_3	Q_2	Q_1	Q_0
t_0	1	0	1	0	1
t_1	1	1	0	1	0
t_2	1	1	1	0	1

(4)

At time t_4?

t_3	1	1	1	1	0
t_4	1	1	1	1	1

(4)

1 mark per correct value