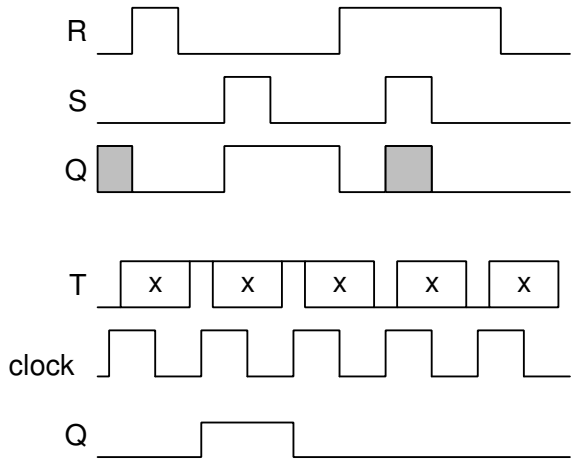
ELEX 2117 : Digital Techniques 2
2020 Winter Term

Practice Quiz 1

Question 1: flip-flops

In the timing diagrams below the shaded areas are "undefined" or "unknown", the areas marked with an × mean "don't care" (these are not the same).

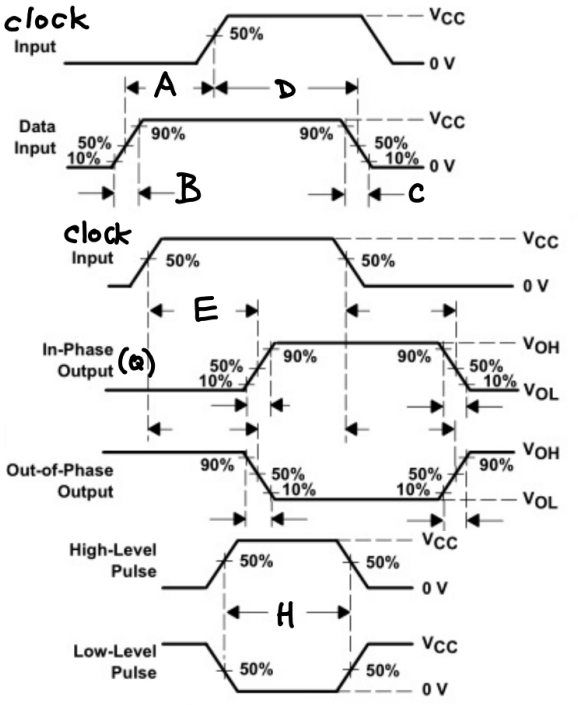


J	K	clk	Q
0	0	↑	Q_0
0	1	↑	0
1	1	↑	$\overline{Q_0}$

The following assumes $\overline{\text{clear}}$ is an asynchronous clear input:

D	$\overline{\text{clear}}$	clk	Q
0	1	↑	0
1	1	↑	1
×	0	×	0
×	1	0	Q_0

Question 2: timing specifications



	description	letter	R/G	min/max
t_{PD}	propagation delay	E[a]	G	max
t_{su}	setup time	A	R	min
t_{co}	clock to output delay	E	G	max
t_H	hold time	D	R	min
T	period	-	-	-
t_r	rise time	B	G[b]	-[c]
t_f	fall time	C	G	-
t_w	pulse width	H	R[d]	-[e]

[a] t_{CO} is a more specific name for a propagation (input-to-output) delay.
[b] t_r and t_f are guaranteed responses for outputs and requirements for an for an input.
[c] Could be either.
[d] If this is an input.
[e] Could be either.

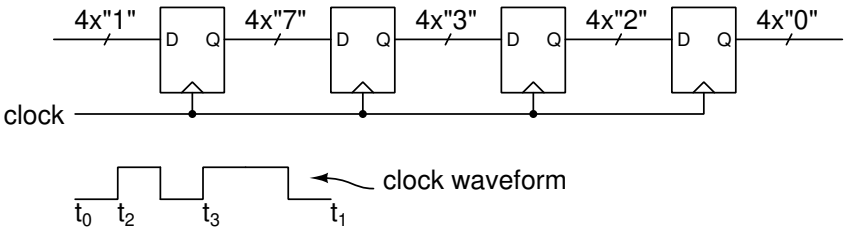
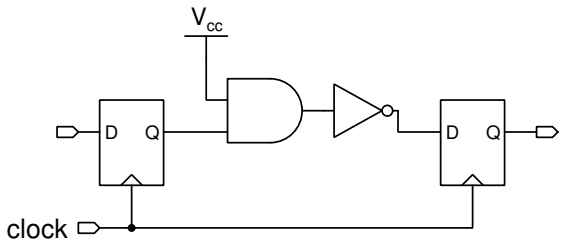


Figure 1: Serial/parallel registers.

Question 3: timing calculations



The constraint on the setup time is that the minimum guaranteed setup time exceed the minimum required setup time:

$$T(\text{min}) - t_{CO}(\text{max}) - t_{PD}(\text{max}) \geq t_{SU}\ (\text{min})$$

The value of the left-hand side is the available setup time while the right-hand side is the required setup time. The designer controls the available setup time by choosing the clock period and combinational logic complexity while the component manufacturer specifies the t_{SU} requirement.

In words, t_{CO}(max) after the "launching" clock edge the signal arrives at the combinational logic. After a further t_{PD}(max) it arrives at the D input of the right flip-flop. This must happen at least t_{SU} (min) before the next ("latching") clock edge which happens a time T after the launching edge.

In the first part of the question, t_{CO} (max) is 3 ns, t_{PD} (max) is 15 ns and t_{SU} (min) is 2 ns. Thus T(min) $\geq$ 2+3+15 = 20 ns and the maximum clock frequency is $1/20\times10^{-9}$ = 50 MHz.

In the second part we are given T(min) = 10 ns (f = 100 MHz), t_{CO} = 3 ns and t_{SU} = 2 ns. Thus $10 - 3 - t_{PD}(\text{max}) \geq 2$ and t_{PD} (max) $\leq$ 5 ns (10 − 3 − 2).

Question 4: registers

Figure 1 shows two rising edges between t_0 and t_1. After each clock edge the flip-flops are loaded with the values on their inputs. Thus the values propagate left to right.

The table below shows the values at the input and at each of the flip-flop outputs at different times.

after	input	FF1	FF2	FF3	FF4
t_0	`4x"1"`	`4x"7"`	`4x"3"`	`4x"3"`	`4x"0"`
t_2	`4x"1"`	`4x"1"`	`4x"7"`	`4x"3"`	`4x"3"`
t_3	`4x"1"`	`4x"1"`	`4x"1"`	`4x"7"`	`4x"3"`