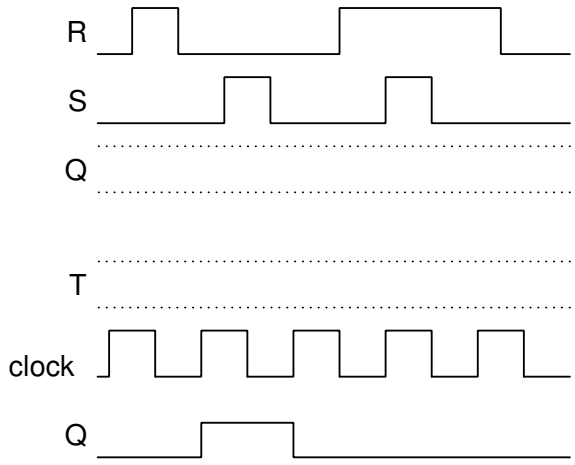
Practice Quiz 1

Question 1: flip-flops

Fill in the missing waveform(s) below. Signals without an overbar are active-high.



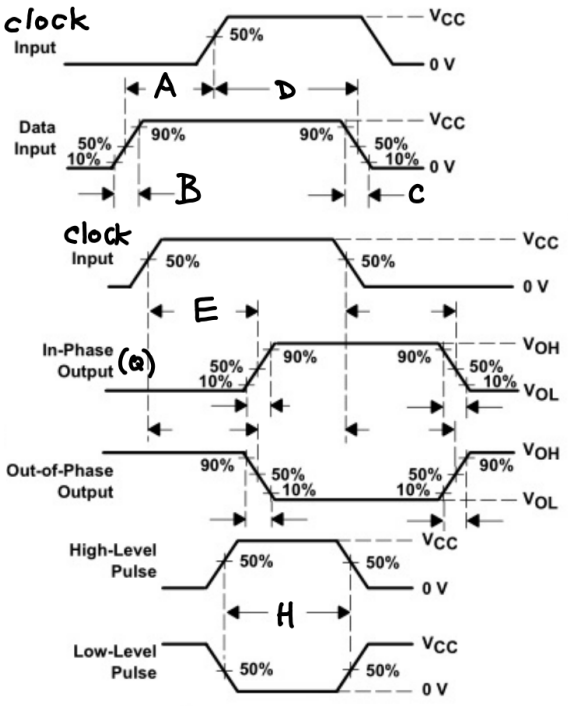
Fill in the missing portions of the following truth tables. Use ↑ for a rising edge, Q_0 for the previous output, and × for "don't care" (meaning this input has no effect).

J	K	clk	Q
		↑	Q_0
		↑	0
		↑	$\overline{Q_0}$

D	$\overline{\text{clear}}$	clk	Q
0	1		0
1	1		1
×	0		
×	1	0	

Note: You should be able to answer this question for RS, D, T or JK flip-flops.

Question 2: timing specifications



	description	letter	R/G	min/ max
t_{PD}	propagation delay			
t_{su}	setup time			
t_{co}	clock to output delay			
t_H	hold time			
T	period			
t_f	rise time			
t_r	fall time			
t_w	pulse width			

Write the letter from the timing diagram above that corresponds to the timing specifications given in each line of the table above. Fill in the "R/G" column with a "G" if the specification is a guaranteed response or "R" if the specification is a timing requirement. Fill

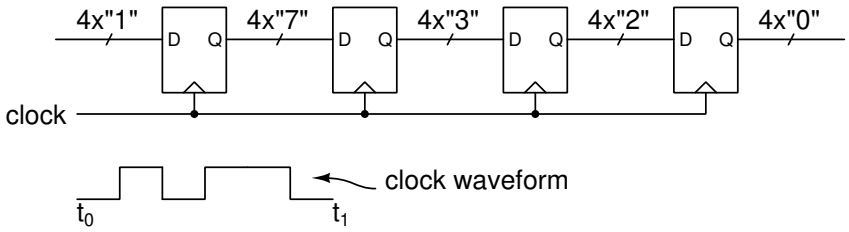
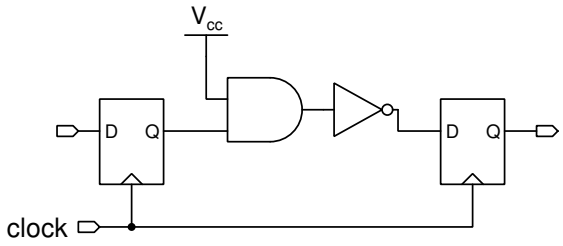


Figure 1: Serial/parallel registers.

in the min/max column with "min" if the specification is most likely to be a minimum or "max" if the specification is most likely to be a maximum. Specifications may appear zero or more times in the diagram.
A "requirement" (R) means the circuit design must ensure this specification is met to ensure correct operation of the device. A "guaranteed response" (G) means the manufacturer guarantees this specification if the device is operated within requirements.

Question 3: timing calculations

In the diagram below, both flip-flops have a t_{CO} of 3 ns and a t_{SU} of 2 ns. The t_{PD} through the combinational logic is 15 ns.



What is maximum clock frequency at which this circuit will operate properly?

If the designer wished the circuit to operate at 100 MHz, what is the maximum allowed propagation delay through the combinational logic?

Question 4: registers

Figure 1 shows four registers and a clock waveform. The contents of the registers at time t_0 are shown at the register outputs (don't worry about the notation, we'll cover that later). The value at the input to the leftmost register is fixed at the value shown.
What are the contents of the registers at time t_1?