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ELEX 2117 : Digital Techniques 2
2020 Winter Term

MIDTERM EXAM 1
9:30 AM – 10:20 AM
Thursday, Feb 27, 2020

This exam has four (4) questions on two (2) pages. The marks for each question are as indicated. There are a total of sixteen (16) marks. Answer all questions. Write your answers and all rough work in this paper and nowhere else. Show your work. Draw a box around your final answer. Numerical answers must include units. Books and notes are allowed. No electronic devices other than calculators are allowed. Show your work.

This exam paper is for:

Sample Exam 1 A000000000

Each exam is equally difficult.

Answer your own exam.

Do not start until you are told to do so.

Name: _____

BCIT ID: _____

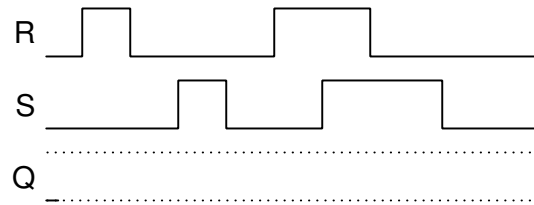
Signature: _____

Question	Mark	Max.
1		6
2		6
3		2
4		2
Total		16

Question 1

6 marks

Fill in the missing waveform below. The initial value of Q is low.



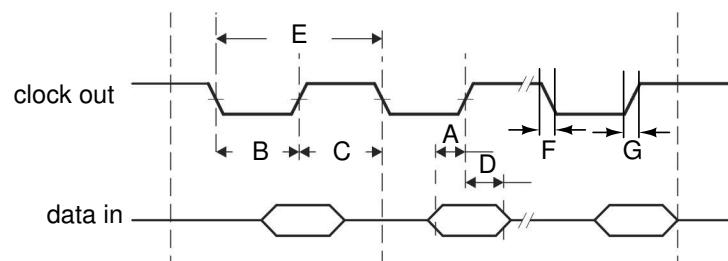
Fill in the missing portions of the following truth table. Use \uparrow for a rising edge, Q_0 for the previous output, and \times for “don’t care” (meaning this input has no effect). $\overline{\text{CLR}}$ is an asynchronous reset.

J	K	$\overline{\text{CLR}}$	clk	Q	\overline{Q}
		0	\uparrow		
		1	\uparrow	0	1
1		1	\uparrow	1	0
		1	\uparrow	$\overline{Q_0}$	Q_0

Question 2

6 marks

This is the timing diagram for the SPI interface of the MSP432 microcontroller¹:



Fill in the following table based on the timing diagram above. For each specification labelled above, give the name of the timing specification (e.g. rise time), the common **variable** name (e.g. t_{SU}). In the “R/G” column place a “G” if the specification is a guaranteed response or “R” if the specification is a timing requirement.

¹You will use this microcontroller in ELEX 3305 next term.

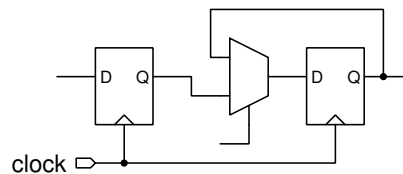
A “requirement” (R) means the circuit design must ensure this specification is met to ensure correct operation of the device. A “guaranteed response” (G) means the manufacturer guarantees this specification if the device is operated within requirements.

letter	name	var.	R/G
A			
$\frac{C}{B+C}$			
D			
E			
F			
G			

Question 3

2 marks

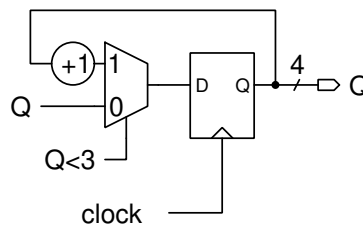
In the diagram below, each flip-flop has a t_{CO} of 5 ns and a t_{SU} of 2 ns. The propagation delay through the multiplexer is 3 ns.



What is maximum clock frequency at which this circuit will operate properly?

Question 4

2 marks



The figure above shows a circuit consisting of a 4-bit register, a multiplexer and an adder that adds 1. The initial value of Q is 0. What are the values of Q after the next four rising edges of the clock?

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This exam paper is for:

Sample Exam 2 A00000000

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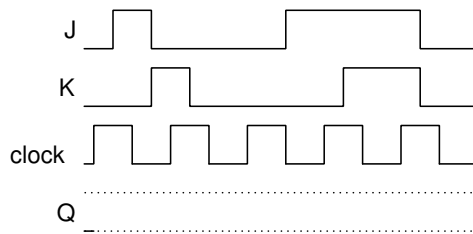
Name: _____
BCIT ID: _____
Signature: _____

Question	Mark	Max.
1		6
2		6
3		2
4		2
Total		16

Question 1

6 marks

Fill in the missing waveform below. The initial value of Q is low.



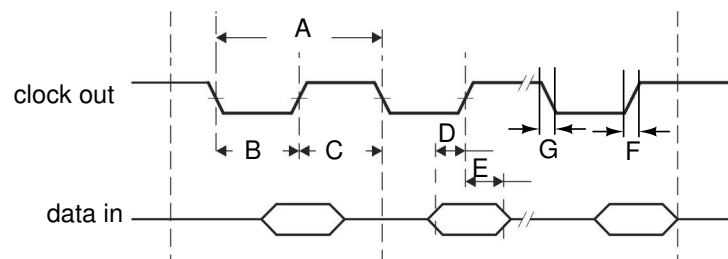
Fill in the missing portions of the following truth table. Use \uparrow for a rising edge, Q_0 for the previous output, and \times for “don’t care” (meaning this input has no effect). $\overline{\text{CLR}}$ is an asynchronous reset.

T	$\overline{\text{CLR}}$	clk	Q	\overline{Q}
	0			
0	1	\uparrow		
	1	\uparrow	$\overline{Q_0}$	
		\uparrow		$\overline{Q_0}$

Question 2

6 marks

This is the timing diagram for the SPI interface of the MSP432 microcontroller¹:



Fill in the following table based on the timing diagram above. For each specification labelled above, give the name of the timing specification (e.g. rise time), the common **variable** name (e.g. t_{SU}). In the “R/G” column place a “G” if the specification is a guaranteed response or “R” if the specification is a timing requirement.

¹You will use this microcontroller in ELEX 3305 next term.

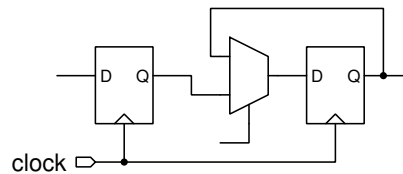
A “requirement” (R) means the circuit design must ensure this specification is met to ensure correct operation of the device. A “guaranteed response” (G) means the manufacturer guarantees this specification if the device is operated within requirements.

letter	name	var.	R/G
A			
$\frac{C}{B+C}$			
D			
E			
F			
G			

Question 3

2 marks

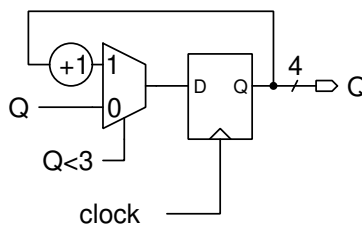
In the diagram below, each flip-flop has a t_{CO} of 3 ns and a t_{SU} of 5 ns. The propagation delay through the multiplexer is 8 ns.



What is maximum clock frequency at which this circuit will operate properly?

Question 4

2 marks



The figure above shows a circuit consisting of a 4-bit register, a multiplexer and an adder that adds 1. The initial value of Q is 1. What are the values of Q after the next four rising edges of the clock?