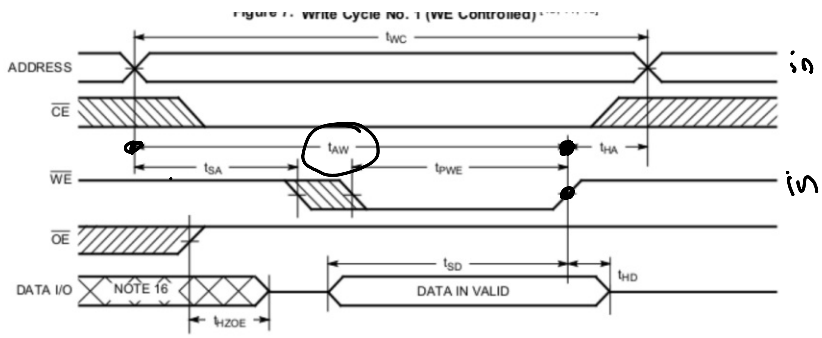
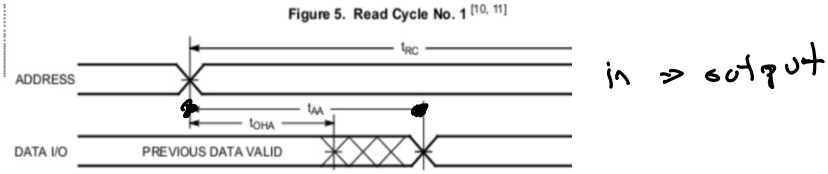
Memory System Design

Exercise 1: Is AW. a requirement or a guaranteed specification for this memory? How about the AA.?



t_{AW} is requirement.

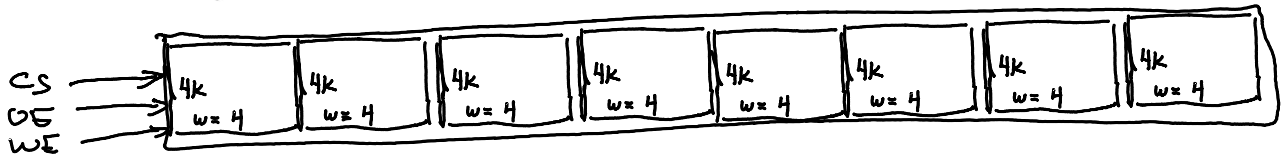
Figure 5. Read Cycle No. 1 [10, 11]

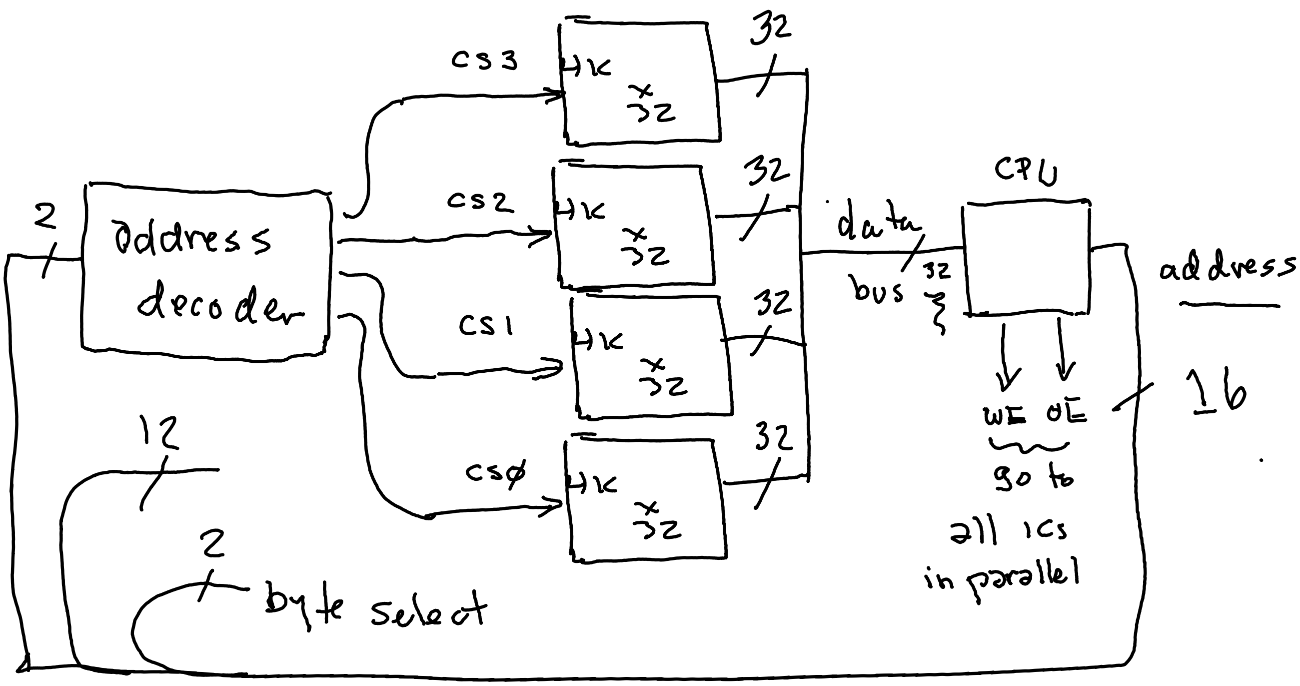


t_{AA} guaranteed specification.

Exercise 2: How many 4 k×4 memory IC's would be required to build a 16 k ×32 memory? What is the width of the data bus? How many address bus bits would be required? What address values could be placed on the address bus? How many chip-select lines would be required?

data bus width = 32 bits





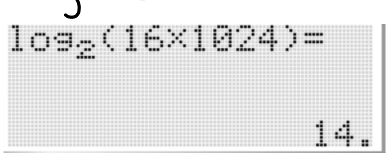
how many bits to address 16k X32?

to select one of 16k words

requires... $2^n = 16k$

$\log_2 2^n = n = \log_2 16k$

using calculator:



$16k = 16 \cdot 1024$

$16k = 2^4 \cdot 2^{10} = 2^{14}$

$\therefore n = 14$

$2^0 = 1$
$2^1 = 2$
2 4 ←
3 8
4 · 16 ←
5 · 32
6 · 64
128
256
512
1024 ←

need 14 bits to select one of 16 K words

this is $16K \cdot \underbrace{\left(\frac{32}{8}\right)}_{4}$ bytes.

need additional 2 bits to select one of 4 bytes in a 32-bit word.

Our addresses have <u>16</u> bits (14 for word, 2 for byte)

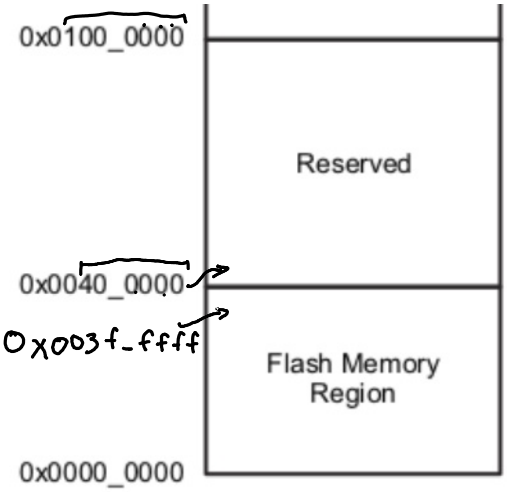
$0 \rightarrow 2^{16}-1$

$\underline{0} \rightarrow \underline{65535}$ to 0 0 0 ..... 0 → $2^{n}-1$ 1 1 1 1 1 1 1

<u>0x</u> 0000 → 0xffff

we have <u>4</u> banks so need <u>4</u> chip-selects.

Exercise 3: How large are the two lowest memory regions in the memory map above?



0x003f_ffff

$2 + 5\times4 = 2+20 = 22$ bits

3f ffff

00	0
01	1
10	2
11	3

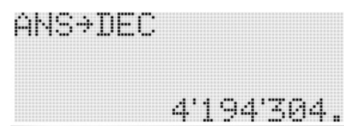
0x 0 0 0 0 0 0 0

first region: $\#\text{bytes} = 2^n = 2^{22}$. $(0 \rightarrow 2^{22}-1$, 0x0 → 0x 3f_ffff$)$

or subtract:

3f_ffff
− 0
+ 1

→ 40_0000_{16} =



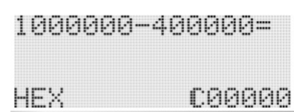
Second region:

100 0000 ← address 1 past end
− 40 0000 ← start

C0 0000

↑ $10_{16} - 4_{16} = 16_{10} - 4_{10} = 12_{10} = C_{16}$

↳ or use calculator



Exercise 4: If a CPU has a 32-bit address bus, now many bytes can it address? What range of addresses would correspond to the first 64 k Bytes? If this range of memory was to be implemented with 32-bit words, how many address bits would be required to select a byte within each word? How many bits would be required to select a 32-bit word within the 64 k range? How many bits are not directly connected to the memory ICs? What are they be used for?

$2^{30} \cdot 2^2 = 2^{10} \cdot 2^{10} \cdot 2^{10} \cdot 2^2$

4 GB.

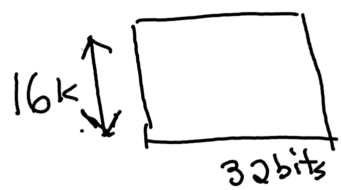
$64 = 64 \cdot 1024$
$= 64 \cdot 1k$
$= 2^6 \cdot 2^{10}$
$= 2^{16}$

32 bits can address 2^{32} bytes.

first 64k bytes:
- $0 - (64k - 1)$ $\quad 0 - 2^{16} - 1$
- $0 -$ 0x10000−1 = 0 − 0xFFFF

- 32 bit words = 4 byte words so need 2 address bits as byte selects.

- 64 k bytes in 4-byte words is $\frac{64k}{4} = 16k$ words

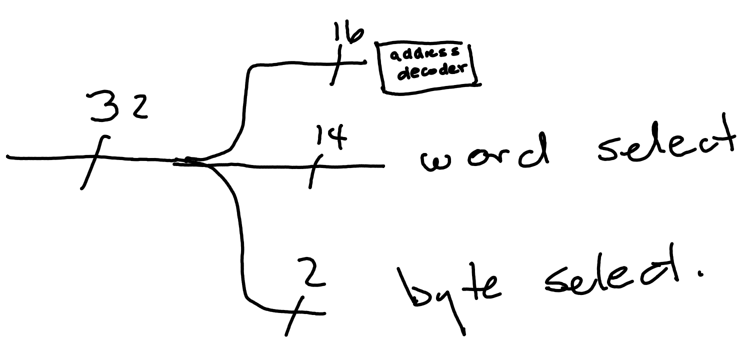


16k × 4 bytes
= 16k × 32 bits.
= 64 k bytes

16×1024
$2^4 \cdot 2^{10}$
2^{14}

$2^n = 16k \quad n = 14$

need 14 bits to select a word.

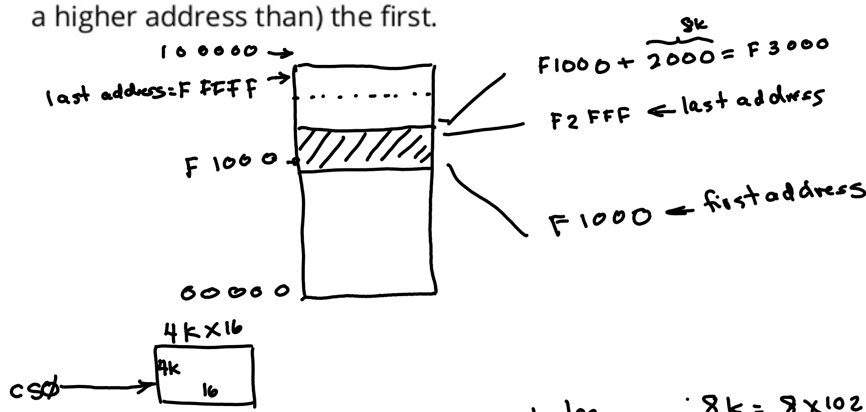


Exercise 5: A 4k×16 memory is to be used in a system with a 20-bit address bus. This memory is to respond to addresses starting at 0xf1000. Draw the memory map. Assuming the address signal is defined as `signal A: std_logic_vector(19 downto 0);` and the chip-select as `signal CS0: std_logic ;`, write the VHDL that would implement the chip-select signal CSO. Write the expression for CS1 if there was a second 4 kB bank immediately above (at a higher address than) the first.

0 – $2^{20}-1$

00000 → FFFFF

F1000



numbers of bytes = 4k · 8 = 8k bytes.

$8k = 8 \times 1024$
$= 2^3 \times 2^{10}$
$= 2^{13}$
$= 2000_{16}$ = 0x2000

$2^0 = 1$
$2^1 = 2$
$2^2 = 4$
$2^{13} = 8192$

CSØ <= '1' when A >= x"F1000" and A < x"F3000" else '0';

or CSØ <= '1' when A ≥ x"F1000" and A ≤ x"F2FFF" else '0';

1111 0001 0000 0000 0000
→ 1111 0010 1111 1111 1111 "don't care"

CSØ <= '1' when A(19 downto 14) = "111100" and
(A(13 downto 12) = "01" or
A(13 downto 12) = "10") else '0';

CS1 <=