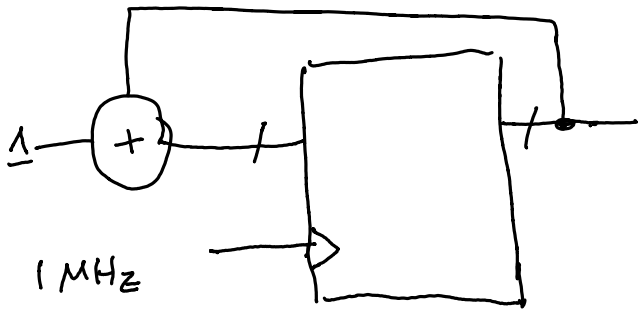
Counters, Timers, State Machines

(see section 7.12 of the text for related material)

Exercise 1: Why do I need to know this?

to do Lab 4
to pass course

Exercise 2: Draw a register with a clock running at 1 MHz. The input comes from an adder that adds 1 to the output. Assume the initial register value is zero.



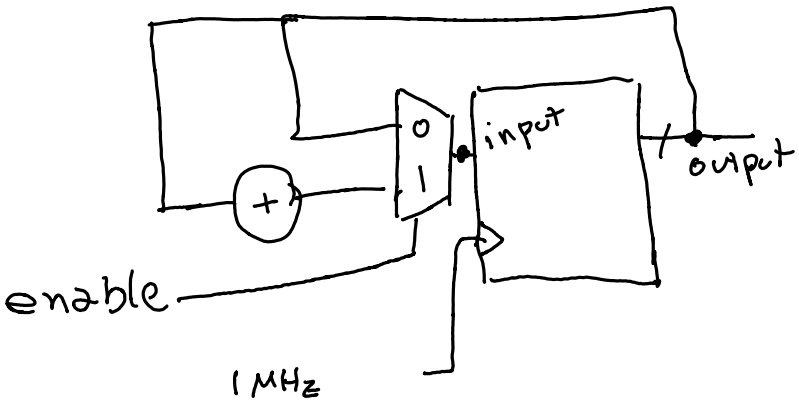
Exercise 3: What values appear at the register output?

0
1
2
3
⋮

Exercise 4: When does the output change?

on rising edge of the clock

Exercise 5: Now add a multiplexer with an enable that selects the output of the adder or the current value of the register.



Exercise 6: What values appear at the output when the enable is asserted? When it is not?

if asserted	if not
0	0
1	0
2	0
3	0
⋮	

Exercise 7: When is the register loaded?

on rising edge of clock

Exercise 8: When is the register loaded with a new value?

if enable is high on " "

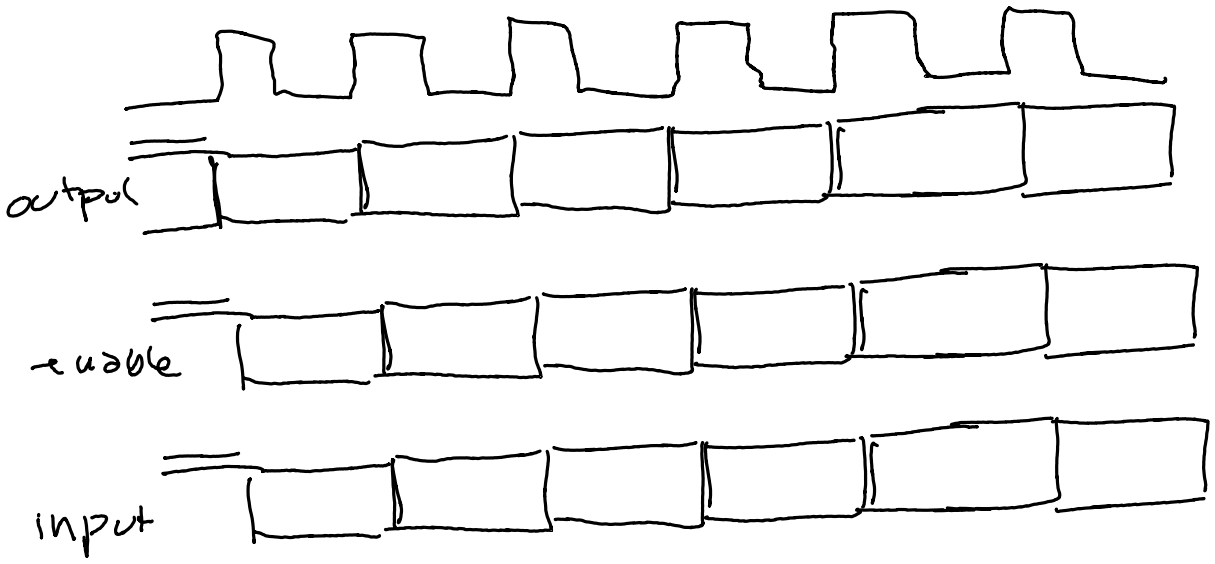
Exercise 9: If the enable lasts for one clock cycle, by how much will the register change?

by 1

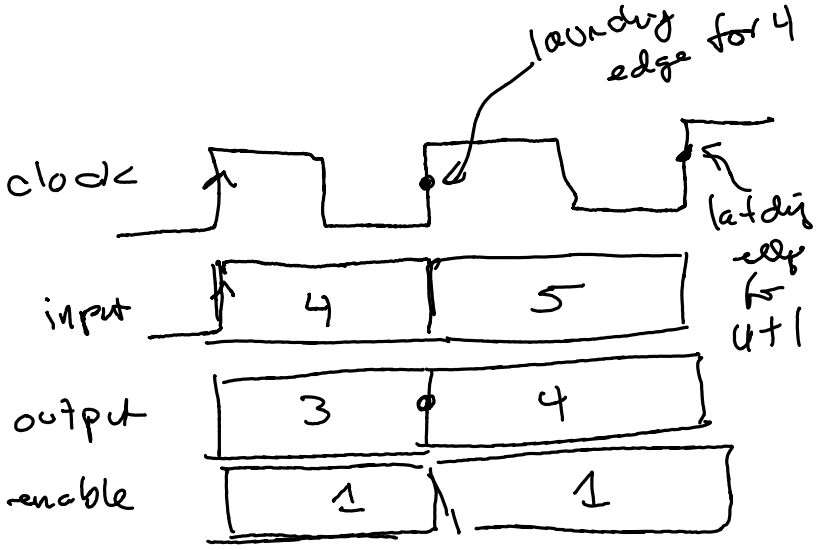
Exercise 10: If the enable is generated as the output of another register, when does it change?

at the same time as this register changes.

Exercise 11: Draw the clock, the enable and the register output as a function of time (ignore propagation delays).



Exercise 12: Label a launching edge. Label the corresponding latching edge. How much time separates them?

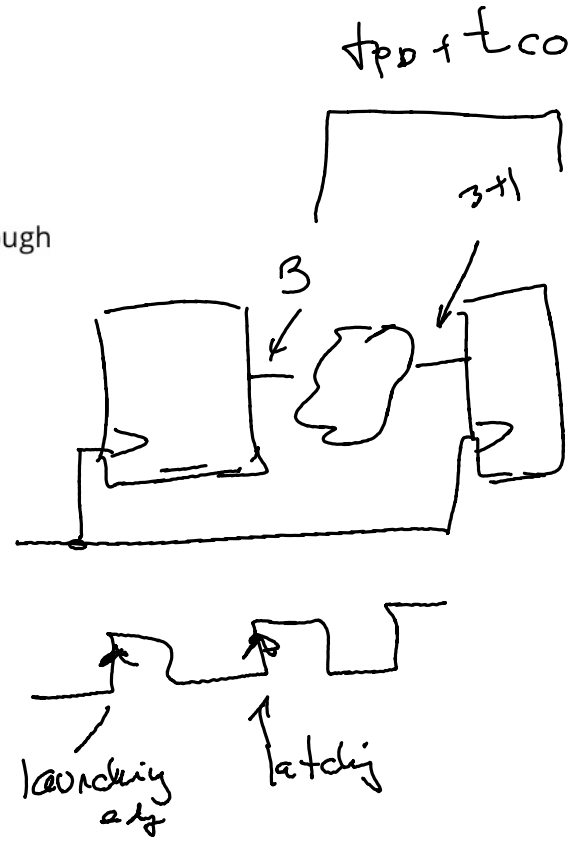


1 period, 1 μs

Exercise 13: How much time is allowed for the signal to travel through the adder and multiplexer?

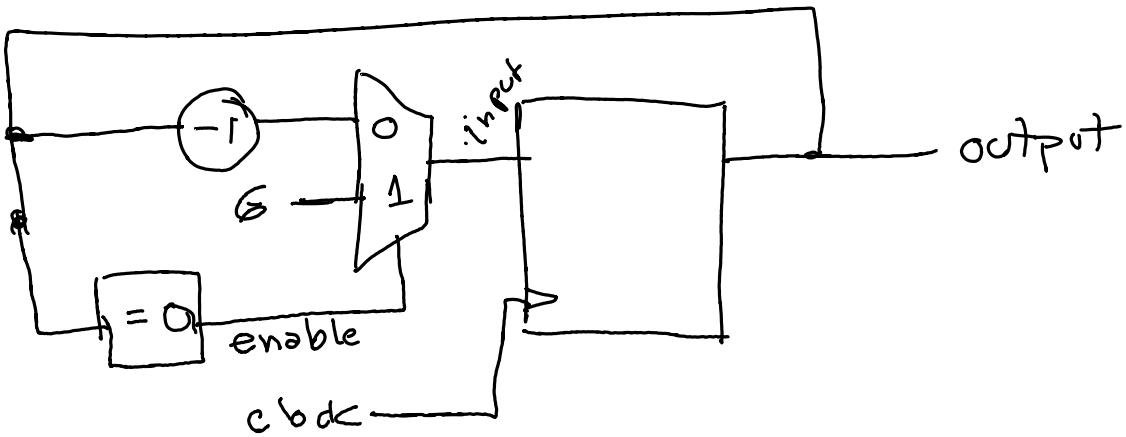
1 clock period

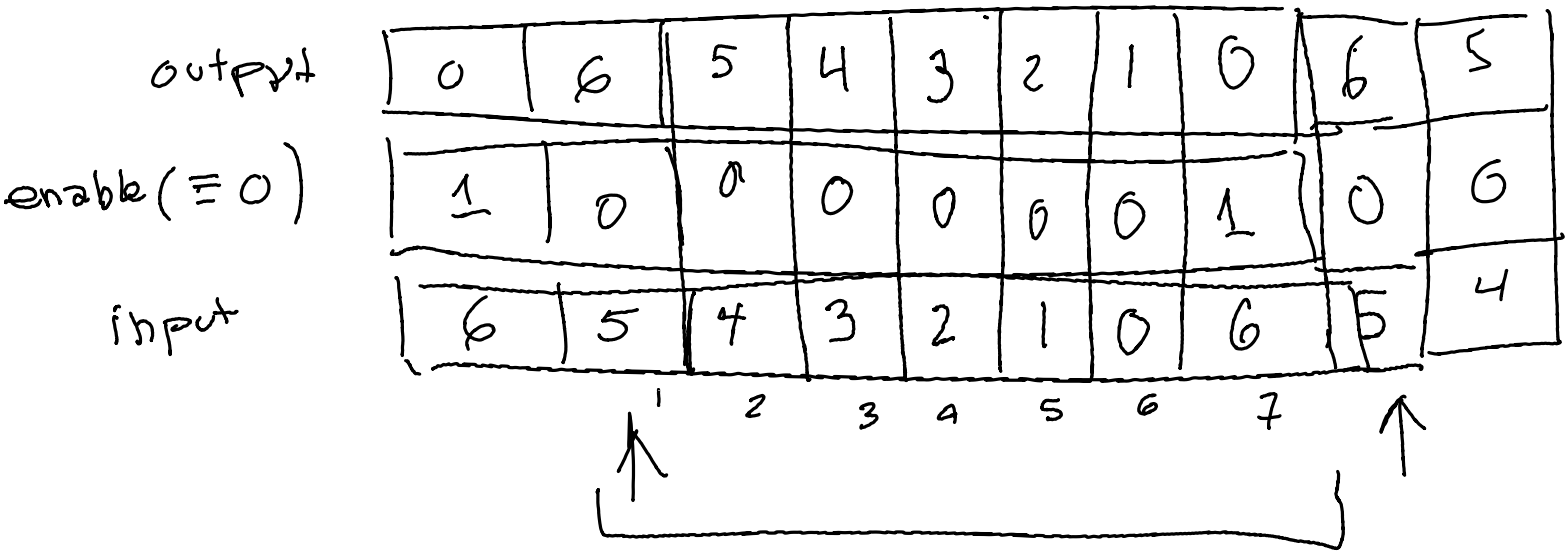
(1 μs)



Exercise 14: What values are produced if we replace the adder with a subtractor, the mux selects between the new value and the value ~~N − 1~~, and the enable is asserted only when the register value is zero?

6





Exercise 15: What is the duration of the zero-detected signal? (enable)

1 clock period

Exercise 16: How often does the counter get reset to ~~$N-1$~~ 6? What is the period? What is the frequency?

every $N = 7$ clock cycles.

$1\mu s \times 7$ clock cycles

$7\mu s$. ≈ 114 kHz

Exercise 17: Why do we call this a timer?

measures clock periods

$\Rightarrow$ measures time.

Exercise 18: Draw the clock, timer values and zero-detect (ignore propagation delays).

(see above).

Exercise 19: Why do we count down and detect zero instead of counting up and detecting some other value?

Exercise 20: How can we detect a zero value without OR'ing all the bits?

Exercise 21: Can we use one timer to control another? What signal do we use?