ELEX 2117 : Digital Techniques 2
2020 Winter Term

Learning Outcomes for Final Exam

This is a list of the questions students should be prepared to answer on the final exam.

Memory Design

- identify the characteristics (volatile or non-volatile, writeable, requiring refresh, byte-erasable, block-erasable, UV-erasable) of common memory technologies (ROM, RAM, SRAM, DRAM, EPROM, EEPROM and flash EEPROM) as well as their relative access times and storage densities
- identify access, setup, hold, period and width timing specifications on timing diagrams of memory read and write cycles
- calculate (byte) memory start/end addresses and region sizes using binary, decimal and hexadecimal notation, including use of (power-of-two) kB, MB and GB units
- determine the number of bits required for byte-select, word-select and bank-(chip)-select given the data bus width, device (IC) memory dimensions and required memory dimensions
- draw a schematic showing how the control (CS, OE, WE), data bus and address bus of an array of memory ICs are connected to increase the data bus width and the total amount of memory
- design address decoding logic in VHDL that asserts a chip-select signal for a specific address range

Interfaces

- distinguish between and explain the advantages and disadvantages of: serial vs. parallel data transfer, synchronous vs. asynchronous, and bidirectional vs. unidirectional interfaces
- determine the waveform (voltage vs. time) appearing at a serial interface's data, clock (if any), and device select (if any) signals when a given value is transmitted
- determine the value transmitted over an interface given a diagram of the waveform transmitted over the interface
- describe purpose of device descriptors

Programmable Logic

- define the following IC terms: VLSI, ASIC, PLD, CPLD, FPGA, LUT, LE, routing, configuration (of a PLD), Xilinx, Intel, wafer, die, fabless, feature size (e.g. 7 nm), NRE
- differentiate between CPLD, FPGA and ASIC technologies in terms of complexity (e.g. number of gates), cost per gate (unit cost), development cost, and development time,
- describe historical trends of transistor feature size (Moores's Law) and its impact on digital vs analog IC complexity and cost
- identify whether a hardware or software solution would be most appropriate for given requirements
- identify whether a custom (ASIC) or programmable (PLD) logic solution would be most appropriate for given requirements

Logic Families

- differentiate between logic levels, numbers, truth values and characters
- given a data sheet, determine: if an input voltage would be high or low or invalid; if an output voltage would be high, low or invalid; the noise margin
- determine the direction of current flow between driver and receiver in the high, low and tri-state output states

- state which transistors are on and off in a totem pole output for high, low and tri-state output states
- identify rise and fall times specifications given a timing diagram
- compute effect of a change in frequency and voltage on the power consumption of CMOS logic circuits