ELEX 2117 : Digital Techniques 2
2020 Winter Term

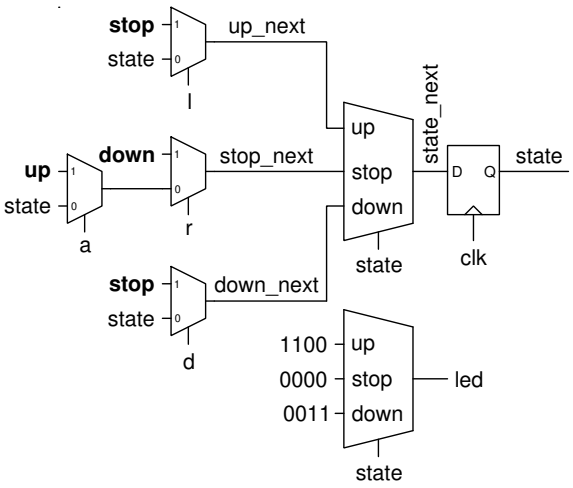
Solutions to Practice Lab Exams

Revision 2: replaced state transition diagrams with block diagrams.

The portions of the **labexam.vhd** file that were added are shown below.

Practice Lab Exam 1

```
type state_t is (up, down, stop ) ;
  signal up_next, down_next, stop_next : state_t ;
  signal state, state_next : state_t ;

...
  -- put your VHDL code here

  up_next <= stop when l = '1' else state ;
  stop_next <= down when r = '1' else
        up when a = '1' else
        stop ;
  down_next <= stop when d = '1' else state ;

  with state select state_next <=
        up_next when up,
        stop_next when stop,
        down_next when down ;

  state <= state_next when rising_edge(clk);

  with state select led <=
        "1100" when up,
        "0000" when stop,
        "0011" when down ;
```



Practice Lab Exam 2

```
type state_t is (s0, s5, s10, s15) ;
signal state, state_next : state_t ;
signal s0_next, s5_next, s10_next, s15_next : state_t ;

...
  -- put your VHDL code here

  s0_next <= s5 when l = '1' else s0 ;
  s5_next <= s10 when l = '1' else s5 ;
  s10_next <= s15 when l = '1' else s10 ;
  s15_next <= s0 when a = '1' else s15 ;

  with state select state_next <=
        s0_next when s0,
        s5_next when s5,
        s10_next when s10,
        s15_next when s15 ;

  state <= state_next when rising_edge(clk);

  with state select led <=
        "0000" when s0|s5|s10,
        "1111" when s15 ;
```