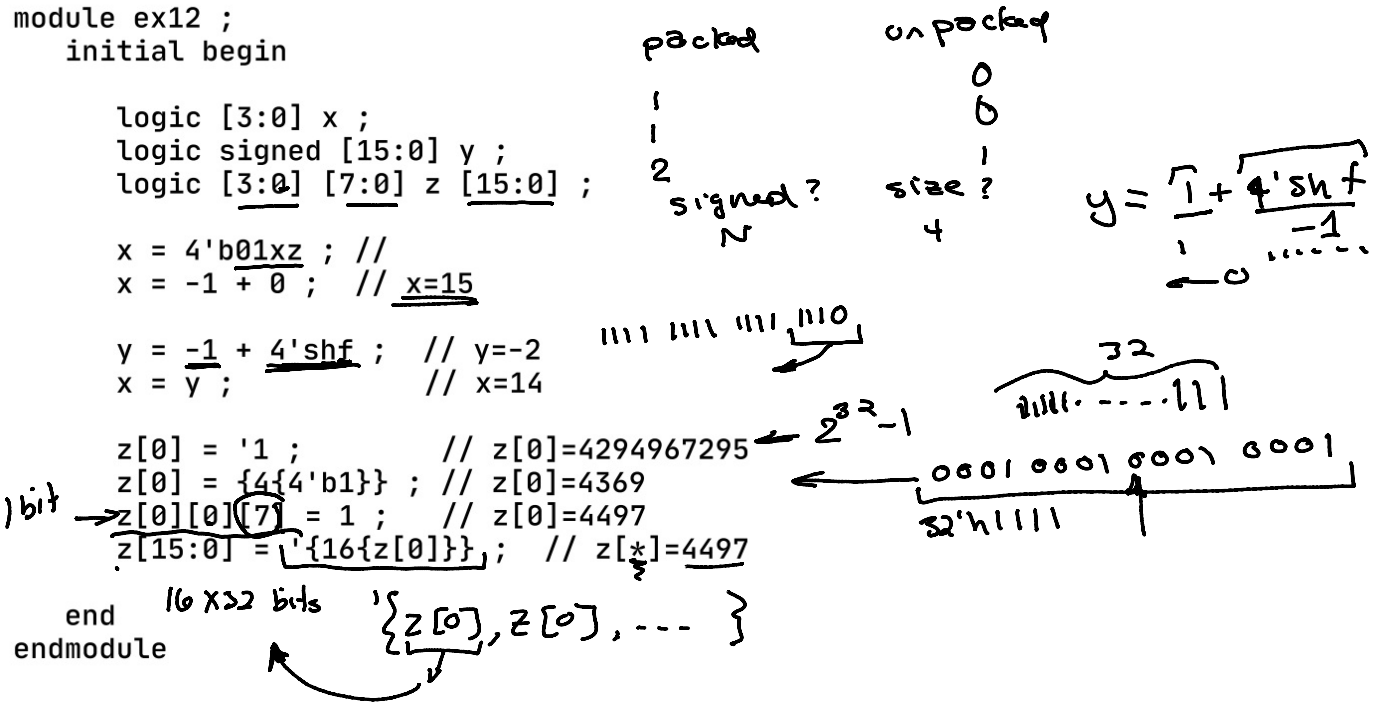
System Verilog

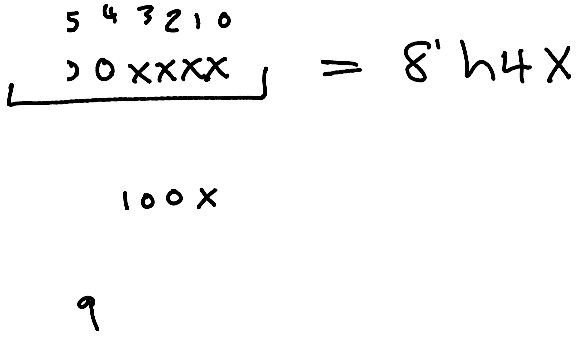
Exercise 1: What are the packed and unpacked dimensions of each declaration?

```
module ex12 ;
   initial begin

      logic [3:0] x ;
      logic signed [15:0] y ;
      logic [3:0] [7:0] z [15:0] ;

      x = 4'b01xz ; //
      x = -1 + 0 ;  // x=15

      y = -1 + 4'shf ;  // y=-2
      x = y ;           // x=14

      z[0] = '1 ;         // z[0]=4294967295
      z[0] = {4{4'b1}} ; // z[0]=4369
      z[0][0][7] = 1 ;   // z[0]=4497
      z[15:0] = '{16{z[0]}} ;  // z[*]=4497

   end
endmodule
```



Exercise 2: What are the signedness, size and value of each constant and each expression above?

```
   initial begin

      logic [15:0] x ;
      logic signed [15:0] y ;

      x = 16'hfff0 ; // x=65520
      y = x >>> 1 ;  // y=0x7ff8
      y = signed'(x) >>> 1 ; // y=0xfff8
      y = |y ; // y=1

      x = 8'h4x ;       // x=X
      y = x == 8'h4x ;  // y=X

     y = x[6:3] === 7'b100x ; // y=1
     y = x ==? 8'h4x ; // y=1
     y = {x[7:4],x[6]} ; // y=0x0009
   end
endmodule
```



Exercise 3: Should each of the following nets (or variables) be declared `wire` or `reg`?

```
module test (a,b,c,d,q) ;
dff d0 (clk,d,q) ; // assume only q is an output
assign d = a & b ;
always@* clk = a & c ;
endmodule
```

clk is reg.

all others wire.