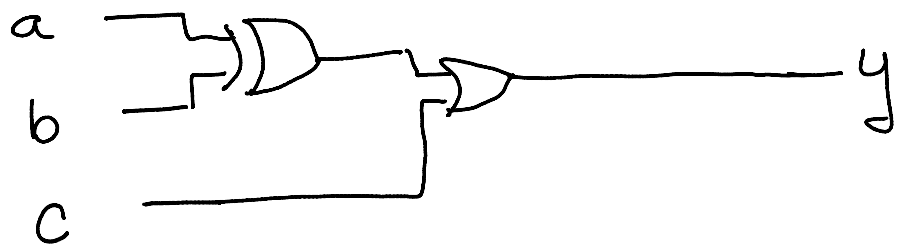
Introduction to Digital Design with Verilog HDL

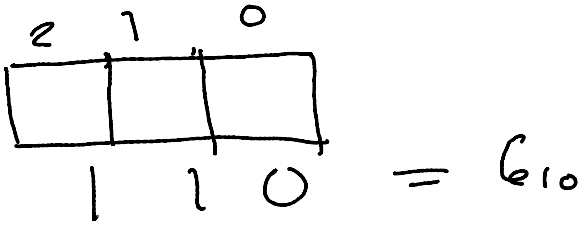
Exercise 1: What changes would result in a 3-input OR gate?

```
// AND gate in Verilog

module ex1 ( input logic a, b, c,
             output logic y ) ;

   assign y = a | b | c ;

endmodule
```

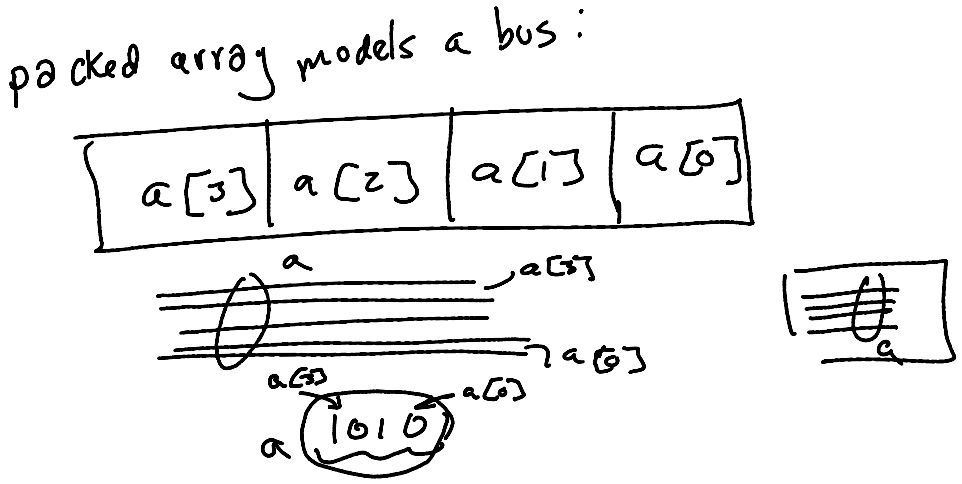
Exercise 2: What schematic would you expect if the statement was `assign y = ( a ^ b ) | c ;`?



Exercise 3: If the signal `i` is declared as `logic [2:0] i;`, what is the 'width' of `i`? If `i` has the value 6 (decimal), what is the value of `i[2]`? Of `i[0]`?

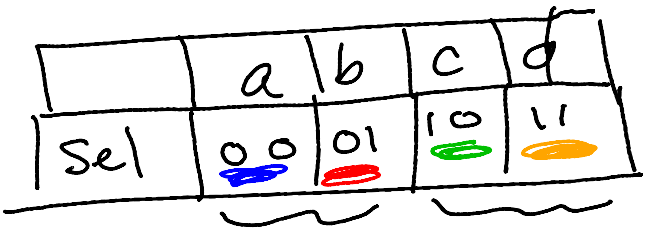


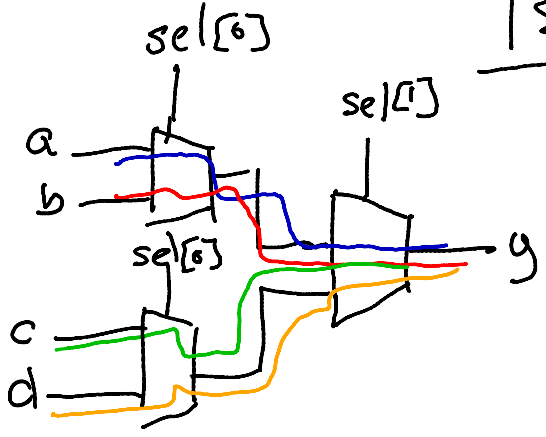
i[2] = 1
i[1] = 1
i[0] = 0



Exercise 4: What changes might result in a 4-bit 4-to-1 multiplexer controlled by a 2-bit `sel` input?

```
1  module ex3 (input logic [1:0] sel,
2              input logic [3:0] a, b, c, d,
3              output logic [3:0] y) ;
4
5     always_comb begin
6       if ( sel[1] == 0 )
7          if ( sel[0] == 0 )
8             y = a ;
9          else
10            y = b ;
11      else
12         if ( sel[0] == 0 )
13            y = c;
14         else
15            y = d ;
16    end
17
18 endmodule
```





Exercise 5: What is the output in binary when the input is a=2'b10

2'b10 = 10

d would be set to 'ha4

32-bit valve (only L.S. 8 bits used)

hA4 = 1010_0100

Exercise 6: What are the values in decimal of the constants in the code above?

8'hC0 , → 1100_0000 = 192

8'b1111_1001 ; →

'ha4 ;

t: d = 176 ; 176