Design Considerations for Sub-mW RF CMOS Low-Noise Amplifiers

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***Abstract*—Design considerations for sub-mW fully integrated narrow-band RF CMOS low-noise amplifiers (LNAs) are presented. The impact of device-level properties and biasing on LNA gain, noise, linearity, and power consumption is discussed. To demonstrate the performance achievable with the design considerations, a cascode LNA is designed in a standard 90nm CMOS process to operate in the 2.4GHz band. The LNA achieves a voltage gain of 22.7dB, NF of 2.8dB, *IIP3* of +5.14dBm, and *P1dB* of -10dBm, while consuming 943µW from a 1V supply.**

I. Introduction

The design of low-power wireless transceivers has gained substantial significance due to the explosion of portable and ubiquitous wireless applications such as personal area networks and wireless sensor networks. These applications demand for small-sized, low-cost, and low-power wireless transceivers with a long battery life. To reduce cost, the use of off-chip elements should be minimized. The first integrated block in most wireless receivers is the low-noise amplifier (LNA). Design considerations for sub-mW fully integrated narrow-band RF CMOS LNAs are described in this paper. The design of a sub-mW CMOS LNA is challenging as a metal-oxide-semiconductor field effect transistor (MOSFET) performs poorly when biased at a small drain current, which is necessary for low-power operation, and the choice of circuit topologies is limited due to the reduction of MOSFET output resistance and supply voltage as technology scales. In addition, on-chip passive elements are of poor quality factor Q and limited range of values. Furthermore, conventional power-constrained noise optimization techniques [1] often lead to subthreshold operation. To optimize for the power and performance of an LNA, this work reviews, coordinates, and exploits several device-level properties: 1) there exists characteristic current densities that yield optimal device transit frequency f_T and unity power gain frequency f_{MAX} [2]; 2) the MOSFET has a large transconductance per unit drain current g_m/I_D in weak inversion [3]; 3) the minimum noise figure decreases as channel length L decreases [2], [4]; and 4) MOSFET linearity improves as drain current density increases, with a significant peaking in the moderate inversion region [5], [6].

This paper is organized as follows. Section II compares circuit topologies and discusses solutions to accommodate small output resistance, low voltage headroom, and on-chip impedance matching. Section III examines the impact of drain current density on LNA gain, noise, and linearity. Section IV presents the design and simulated performance of a sub-mW LNA. Section V concludes the paper.

II. Circuit Topology

The key specifications for characterizing the performance of an integrated LNA are gain, noise, linearity, power consumption, stability, and input matching. These specifications depend on the circuit topology. Compared to the common-source LNA, the common-gate LNA is more suitable for wide-band operation but suffers from relatively high noise figure (NF) [7]. Since the focus of this paper is on narrow-band applications, common-source would be a good choice. However, it suffers from the following shortcomings. 1) Poor isolation between input and output, due to the gate-to-drain parasitic capacitance C_{gd}, increases the chance of instability significantly. Stability can be ensured by designing the LNA such that it satisfies Rollett's stability criteria [8]. Verifying the circuit against the criteria is in practice rather computationally intensive. 2) As CMOS technology scales, the MOSFET output resistance r_o decreases, causing noticeable performance degradation. For a common-source amplifier, r_o appears in parallel with the load impedance in small-signal operation, decreasing the output impedance, and lowering the gain of the LNA. A possible solution is to increase the gate length L, which results in significant NF degradation.

To alleviate the shortcomings of the common-source topology, the cascode topology of Fig. 1(a) is often used. The cascode amplifier consists of an input transistor M_1 and a cascode transistor M_2 with a gate bias voltage V_B. Since the cascode amplifier consists of two stacked transistors, the load should not consume a large voltage headroom. An inductive load L_d, as opposed to a resistive load, is preferred. An inductive load has the added benefit of

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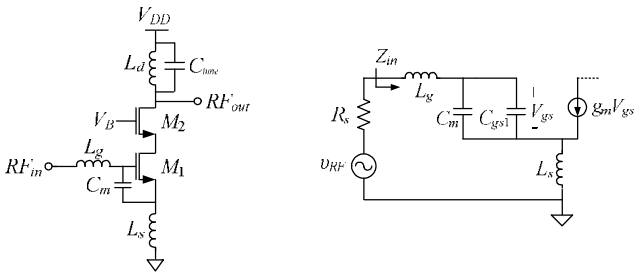


(a) (b)

Figure 1. (a) Schematic of a cascode amplifier. (b) Simplified small-signal model for input matching analysis.

increasing the gain by resonating with the capacitances associated with the output node.

An LNA must provide an input matching to a typically 50Ω element such as a band-select filter or an antenna. In a fully integrated receiver, LNA output matching is often not required as it is connected on-chip to the next stage in the receive chain. However, to minimize the number of off-chip components, a monolithic LNA should implement the input matching network on-chip. One popular approach is to use inductive degeneration. Fig. 1(b) is a simplified small-signal model showing the components for input matching, where C_{gs1} denotes the parasitic gate-to-source capacitance of M_1. The input impedance of the LNA Z_{in} can be expressed as

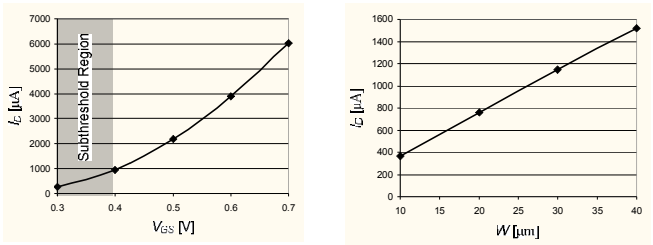
$$Z_{in} = \frac{1}{j\omega C_{gs}} + j\omega(L_s + L_g) + \frac{g_m L_s}{C_{gs}} \tag{1}$$

where g_m is the small-signal (low-frequency) transconductance and $C_{gs} = C_m \parallel C_{gs1}$ is the combined gate-to-source capacitance. Since Z_{in} is to be matched to 50Ω, we have:

$$\Re e\{Z_{in}\} = \frac{g_m L_s}{C_{gs}} = R_s = 50\Omega \tag{2}$$

$$\Im m\{Z_{in}\} = \frac{1}{\omega C_{gs}} + \omega(L_s + L_g) = 0 \tag{3}$$

Since on-chip inductors have a limited range of values for which the Q is reasonable, the capacitor C_m of Fig. 1(a) is added between the gate and source terminals of M_1 so that the values of L_g and L_s are reduced to permit on-chip implementation. Reducing the inductor value also improves Q, which reduces input losses and improves LNA NF. Adding C_m has another advantage of providing an extra degree of freedom for choosing the gate width W of M_1, which decouples impedance matching requirements from power consumption requirements. A drawback of adding extra gate-to-source capacitance is the degradation of f_T of M_1. However, as discussed subsequently, at operating frequencies well below f_T, this tradeoff is reasonable. It is also interesting to note that adding C_m does not degrade distortion performance [6].



(a) (b)

Figure 2. Drain current of a cascode LNA. (a) I_D vs. V_{GS} (W_1=W_2=25μm), (b) I_D vs. W (V_{GS}=0.4V).

III. Power-Aware Design

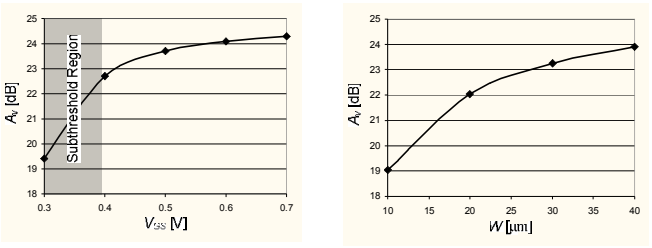
The biasing of the transistors, characterized by the drain current I_D, has strong implications on LNA performance such as gain, noise, and linearity. When a short-channel MOSFET is biased in saturation, I_D can be expressed by

$$I_D = W v_{sat} C_{ox} \frac{(V_{GS} - V_{TH})^2}{(V_{GS} - V_{TH}) + E_c L}(1 + \lambda V_{DS}) \tag{4}$$

where $v_{sat} \approx 10^7$cm/s is the saturation velocity and E_c is the critical field ($E_c \approx 6\times10^4$ V/cm for electrons and 24×10^4 V/cm for holes). As shown by (4), when L is kept to its minimum, V_{GS} and W are key design parameters that directly link to power consumption. The drain current of a 90nm cascode LNA is plotted in Fig. 2 to quantify the sensitivity of power consumption to V_{GS} and W (supply voltage = 1V). Fig. 2(a) depicts the drain current of a cascode LNA with both transistors sized to 25μm. The threshold voltage of the technology used is around 0.4V. In the typical analog design space for this technology (i.e., V_{GS} in the range of 0.4V to 0.7V), power consumption increases 6.4× whereas, in Fig. 2(b) a change of W from 10μm to 40μm (V_{GS} held constant at 0.4V) leads to a power increase of 4.2×. It is interesting to note that, given a drain-to-source voltage, the performance of the MOSFET is strongly tied to the drain current density I_D/W, which can only be modified by V_{GS} but not by W. The following subsections describe the sensitivity of gain, noise, and linearity to V_{GS} and W.

A. Gain

In conventional RF and microwave design approaches [9], [10], primarily developed for high-speed bipolar circuits, f_T and f_{MAX} are two indispensable design parameters. For CMOS technologies, as empirically shown in [2], there exists two characteristic current densities, both associated with operating in strong inversion, that yield optimal f_T and f_{MAX}. For the 90nm CMOS technology used, $V_{GS} \approx 0.7$V is required to reach these optimal values.



(a) (b)

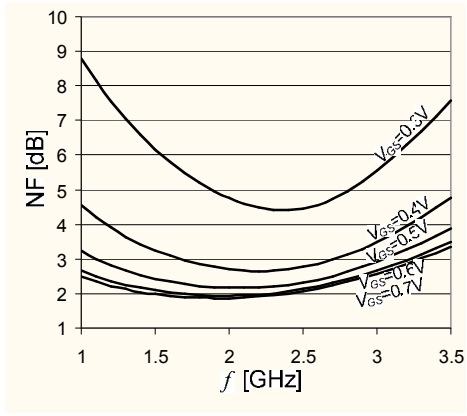
Figure 3. Voltage gain as a function of design variables. (a) A_v vs. V_{GS}, (b) A_v vs. W.

Fig. 3(a) shows the simulated voltage gain A_v of the cascode amplifier depicted in Fig. 1(a) at 2.4GHz. While sweeping V_{GS}, V_B is also modified such that the ratio V_{GS1}/V_{GS2}, hence g_{m1}/g_{m2}, is relatively constant. It may seem counterintuitive that A_v only increases slightly as V_{GS} changes from 0.4V to 0.7V, which corresponds to doubling f_T. For comparison, Fig. 3(b) shows moderate increase in A_v as the widths of both transistors are increased.

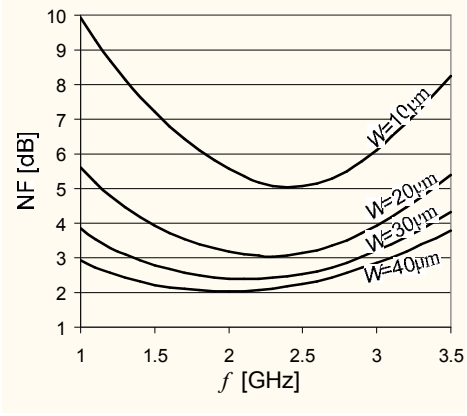
Why does the voltage gain seem insensitive to V_{GS}? The reason lies in the fact that the operating frequency is sufficiently low compared to the maximum f_T of the technology. The transconductance of a transistor has a low-pass behavior. After the cutoff frequency, which marks the bandwidth of the transistor, transconductance rolls off. Since the device becomes less power efficient when biased for a high f_T, to save power, the device should be biased with a bandwidth that is just sufficient for the operating frequency.

B. Noise

According to classical noise theory, for a two port system, there is an optimal source impedance that can minimize the NF of the system. Equivalently, design parameters within the LNA should be chosen such that its noise impedance is matched to the 50Ω input source. A number of LNA design optimization techniques are well established such as classical noise matching (CNM), simultaneous noise and input matching (SNIM), power-constrained simultaneous noise and input matching (PCSNIM), and power-constrained noise optimization (PCNO). A good overview of these techniques is presented in [1]. In particular, PCNO and its variants have been proposed to target low-power design. This technique is based on first finding an optimal gate width, then biasing the device with the amount of drain current allowed by the power constraint. In sub-mW designs, the large optimal gate width combined with a small drain current often force the device to be biased in the subthreshold region. When subthreshold operation is inadequate, such as insufficient frequency response, the technique is no longer applicable.



(a)



(b)

Figure 4. NF of cascode LNA. (a) NF vs. V_{GS}, and (b) NF vs. W.

In the absence of a robust noise optimization technique specifically developed for the sub-mW regime, an alternative design approach could be to determine the sensitivity of NF with respect to V_{GS} and W. For this purpose, a 90nm cascode LNA is simulated. Fig. 4(a) shows NF as V_{GS} of M_1 is swept from 0.3V to 0.7V (W=25µm). V_B is adjusted accordingly as mentioned earlier. As can be seen from Fig. 4(a), NF is inadequate when operating in the subthreshold region (V_{GS} = 0.3V). For a change of V_{GS} from 0.4V to 0.7V, NF is reduced by 0.6dB in the expense of 6.4× the power consumption. Fig. 4(b) shows NF as the width of both transistors are changed simultaneously from 10µm to 40µm (V_{GS} = 0.4V), which results in a 3.4dB NF improvement in the expense of 4.2× the power consumption. This suggests that increasing W is a more effective method for reducing NF.

It is also instructive to use the SpectreRF simulator to obtain a noise summary that shows the noise contribution of components. Fig. 5 depicts the RF signal source and the LNA with the inductor models explicitly shown. The noise contribution from inductor parasitic resistances is significant, suggesting high-Q inductors are highly desirable.

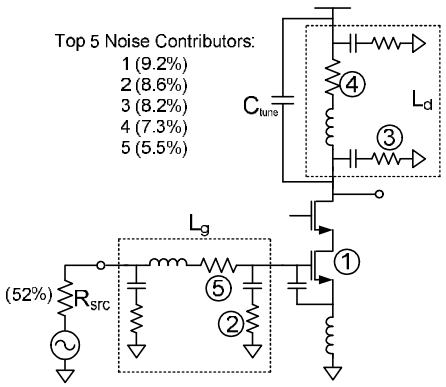
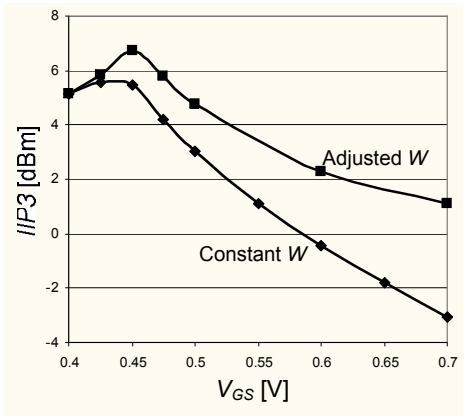
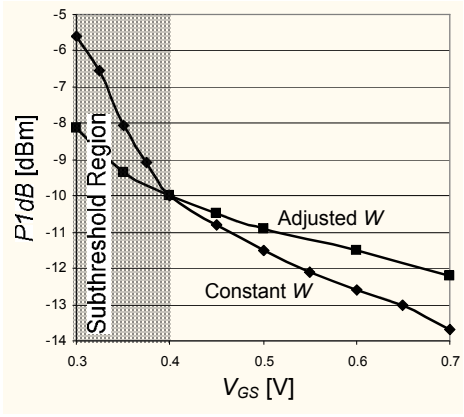


Figure 5. Noise contribution of the signal source and LNA components.



(a)



(b)

Figure 6. Linearity performance of cascode LNA. (a) *IIP3* vs. V_{GS}, and (b) *P1dB* vs. V_{GS}.

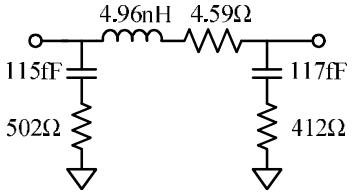


Figure 7. π-model of a 5nH spiral inductor.

C. Linearity

There are two types of linearity performance for an LNA. Small-signal linearity, characterized by the input-referred 3rd-order intermodulation intercept point *IIP3*, is crucial to prevent the intermodulation tones created by a large interfering signal from corrupting the signal of interest. Large-signal linearity, characterized by the input-referred 1dB voltage compression point *P1dB*, is important as it determines the upper bound of the dynamic range of the LNA.

Fig. 6(a) and (b) respectively show the *IIP3* and *P1dB* of a cascode LNA with 25µm transistors. Since linearity is a function of gain, Fig. 6 also show the linearity of the LNA with gate widths adjusted to maintain a constant gain across V_{GS}. V_B is adjusted accordingly as mentioned earlier. The *IIP3* and *P1dB* of the LNA degrade as V_{GS} increases. This is an interesting observation since previous analysis and measurements reveal that the MOSFET *IIP3* performance improves as V_{GS} increases, with a significant peaking in the moderate inversion region [5], [6]. However, it has been reported that linearity of a MOSFET in moderate inversion is not well studied [5] and that the *IIP3* peaking for a CMOS short-channel transistor may not be easily applicable for RF LNA designs [6]. This is due to the fact that source degeneration tends to improve the overall linearity but dampen the peak.

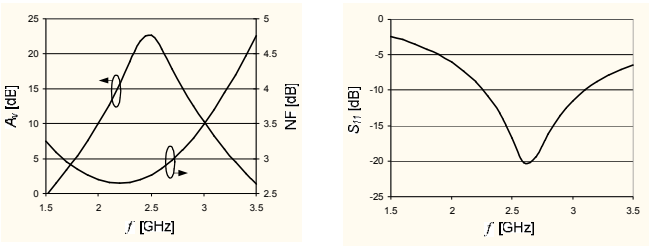
IV. Simulation Results

To demonstrate the application of the above design considerations, an LNA is designed and simulated in a commercial 90nm CMOS technology to operate at the 2.4GHz band. The circuit consumes 943µW from a 1V supply.

Inductors are modeled and designed using ASITIC [11]. Fig. 7 depicts the π-model for a 5nH spiral inductor used as L_g and L_d in Fig. 1(a), implemented using the thick metal layer of a 90nm technology. This inductor has a Q of 7.3. To further improve Q, two metal layers can be used to reduce the series resistance of the inductor. L_s is modeled similarly.

C_m and C_{tune} are implemented using high-Q metal-insulator-metal (MIM) capacitors. The widths of both transistors are sized equally. V_{GS} is chosen to be 0.4V, slightly above the threshold voltage to exploit the high g_m/I_D in moderate inversion. Table 1 is a summary of component values.

Fig. 8 shows the voltage gain, S_{11}, and NF of the LNA. The voltage gain is 22.7dB in the 2.4GHz band with a 3dB bandwidth of around 300MHz. An S_{11} of -14.7dB provides a good input impedance matching to 50Ω. NF is 2.8dB which is acceptable for short-range applications. *IIP3* and *P1dB* are 5.14dBm and -10dBm, respectively. Table 2 shows a performance comparison between the proposed LNA and sub-mW CMOS LNAs from recent literature.



(a) (b)

Figure 8. Performance of the proposed LNA. (a) Gain and S_{11}, and (b) NF.

TABLE 1
SUMMARY OF LNA COMPONENT VALUES

V_{DD} (V)	1
$L_g = L_d$ (nH)	5
L_s (nH)	2
C_m (fF)	480
C_{tune} (fF)	720
W_1/L_1 (μm)	25/0.1
W_2/L_2 (μm)	25/0.1
$V_{in,DC}$ (V)	0.4
V_B (V)	0.9

TABLE 2
COMPARISON OF CMOS LOW-POWER LNAS

	This work	[12][1,#]	[13][2,#]	[14][#]	[15][#]
Gain (dB)	22.7	13.6	13*	12	9.2*
NF (dB)	2.8	4.6	3.6	1.8	3.6
S_{11} (dB)	-14.7	-5	<-10	-18	-10
IIP3 (dBm)	5.14	7.2	-10	-3	-7.25
P1dB (dBm)	-10	-0.2	–	–	-15.8
P_{DC} (μW)	943	260	720	900	1000
f_c (GHz)	2.4	1	0-0.96	2.4	5.5
Gate L (μm)	0.09	0.18	0.13	0.18	0.09

* Power gain, [1] Subthreshold design, [2] UWB design, [#] Measurement

V. CONCLUSION

Design considerations for sub-mW fully integrated RF CMOS LNAs are presented with an emphasis on the tradeoff between gain, noise, linearity, and power consumption. A 2.4GHz 90nm cascode LNA is designed to demonstrate good performance achievable in the microwatt range. For designs that operate well below f_T, the transistor can be biased just above the threshold voltage to exploit the high g_m/I_D, achieving low power consumption, while avoiding the performance degradation associated with the subthreshold region. This observation is significant as many RF applications operating in the low-GHz range implemented in a modern CMOS technology can be designed this way.

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