On the Design of mm-Wave Self-Mixing-VCO Architecture for High Tuning-Range and Low Phase Noise

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***Abstract*—Frequency synthesis at mm-wave range suffers from a severe tradeoff between phase noise (PN) and frequency tuning range (FTR). This work presents the analysis and compares the performance of fundamental-mode voltage-controlled oscillators (F-VCOs) to harmonic-mode VCOs (H-VCOs). It is shown that unlike a mm-wave F-VCO, an H-VCO can simultaneously achieve higher FTR and lower PN. An H-VCO architecture, denoted as self-mixing VCO (SMV), is presented where the VCO core generates both the first (f_0) and second harmonic $(2f_0)$ and then mixes them together to obtain the desired mm-wave third-harmonic $(3f_0)$. Use of a Class-C push–push topology as the VCO core enhances the second-harmonic content to improve mixing efficiency, decreases parasitic capacitance, and improves PN. Compared to an F-VCO operating in a mm-wave band at a fundamental frequency that equals $3f_0$, the proposed SMV architecture achieves about $2\times$ higher FTR and a better PN performance. A 52.8–62.5 GHz SMV prototype is designed and implemented in a 0.13 μm CMOS process. Measurement results show that the VCO achieves an FTR of 16.8% with a PN of -100.6 dBc/Hz at 1 MHz offset—resulting in an FTR-inclusive figure-of-merit (FoM_T) of -190.85 dBc/Hz while consuming 7.6 mW from a 1.2 V supply.**

***Index Terms*—60 GHz, Class-C, harmonic oscillator, high tuning range, local oscillator (LC)-VCO, low phase noise (PN), mm-wave, self-mixing voltage-controlled oscillator (VCO).**

I. Introduction

THE availability of wide bandwidth in the mm-wave portion of the frequency spectrum makes these bands attractive for high-data-rate applications such as wireless high-definition video streaming and medical imaging [1]–[4]. One of the main challenges in most communication systems operating in the 60 GHz and higher frequency bands is to synthesize an on-chip local oscillator (LO) with a high spectral purity and a large tuning range. In addition, when incorporated into a phase-locked loop (PLL), this LO signal needs a mm-wave divider which is challenging to design, and can consume more than 70% of the PLL power budget [4].

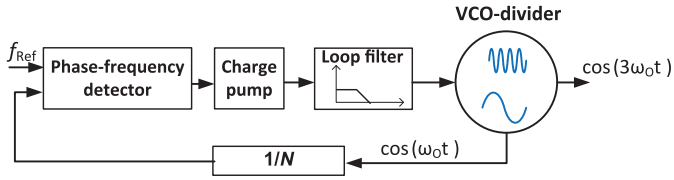

Fig. 1. Application of H-VCO in a PLL.

The signal synthesis techniques can be broadly classified into direct and indirect synthesis, based on whether the desired LO frequency is the same as the voltage-controlled oscillator (VCO) fundamental (f_0), or higher than f_0, respectively. At mm-wave frequencies, direct LO synthesis techniques face several design challenges to meet the desired PN and tuning-range requirements. First, as f_0 approaches the maximum oscillation frequency $(f_{\max})$ of the transistors in a given process technology, the available power gain of transistors degrades. Thus, an excess power is required to guarantee a sustained oscillation. Second, the quality factor (Q) of passive devices (capacitors, varactors, and inductors) implemented on a lossy silicon substrate degrades significantly in mm-wave region and adversely impacts the PN performance and start-up power requirement. Third, the parasitic capacitance of the oscillator active core, interconnects, and output buffer stage (C_{par}) become a significant fraction of the total tank capacitance, thereby permitting only a small MOS varactor (C_{var}) to be used for frequency tuning. Frequency tuning range (FTR) being proportional to C_{var} and inversely proportional to C_{par}, is therefore significantly limited [1]–[3]. Fourth, the switched-tuning technique [5] is no longer effective for reducing the VCO gain, K_{VCO} (defined as the derivative of VCO output frequency to its input control voltage), since switches add more parasitic capacitance and loss to the tank. With most of the tank capacitance contributed by the transistors and varactors, more AM–PM conversion will be observed in the mm-wave VCO owing to the nonlinearity of the MOS capacitor, degrading the PN of VCO. Furthermore, with a large K_{VCO}, the amplitude noise of the tank and the active elements in the oscillator core can also impact the PN [5], [6]. In addition, using a large K_{VCO} in a PLL would result in increasing the reference spur.

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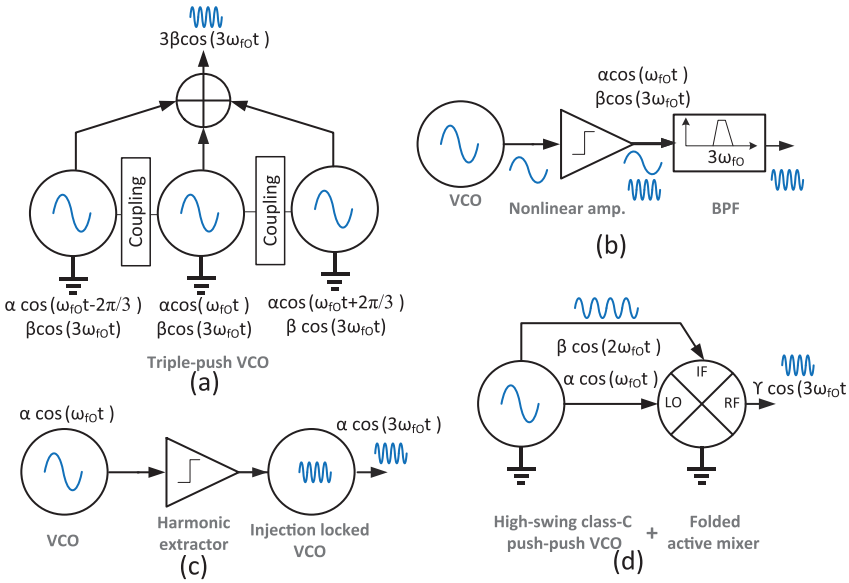

Fig. 2. Indirect LO synthesis techniques for H-VCOs. (a) Triple-push VCOs with third-harmonic summation [3]. (b) VCO followed with third-harmonic generation and band-pass filtering [10]. (c) VCO followed with third-harmonic extraction and injection-locking. (d) SMV with first- and second-harmonic mixing.

To address above-mentioned challenges in cross-coupled fundamental-mode VCOs (F-VCOs), several interesting techniques have been proposed recently. In [7], the quality factor of the LC tank Q_{tank} is increased by reducing the size of the varactor and the VCO frequency is tuned by using the body effect which can adjust the drain capacitance of the MOS device. Although a higher Q_{tank} results in a better PN performance, FTR is limited (4.5%) due to the small size of the varactor. An effective method of increasing FTR and to cover a large range of frequencies is to use a dual-mode LC-tank—up to 28% of FTR is achieved in [8]. However, due to the use of a complex inductor structure, Q_{tank} is sacrificed which deteriorates the PN performance. To improve the PN performance while still utilizing an explicit MOS varactor, inductive peaking at the gate of MOS devices is used to increase the $f_{\max}$ and the transconductance of the cross-coupled pair [2]. Although achieving a reasonable tradeoff of PN, power consumption and FTR ($<9\%$), a larger FTR ($>10\%-15\%$) is still desirable.

Indirect LO synthesis techniques using harmonic-mode VCO (H-VCO) generate and utilize higher order harmonics. The benefits of this approach include increased FTR and ease of implementation in a PLL by relaxing the frequency constrains for the divider as shown in Fig. 1 [4], [9]. Fig. 2(a) shows a triple-push-VCO structure [3] where f_0 and $3f_0$ generated by three VCOs are added destructively and constructively, respectively. Although this technique achieves a large FTR at 60 GHz, extensive electromagnetic simulations of the nested-inductor and tank layouts are needed and any error modeling in coupling factors may alter the center frequency, degrade the Q, and adversely affect the PN [3]. Furthermore, improving the PN performance requires higher selectivity at f_0, thereby reducing the power of the desired $3f_0$ harmonic. Finally, due to the use of multiple oscillators, a relatively large dc power is consumed. Fig. 2(b) shows another technique [10] where a large signal swing at f_0 generated by the VCO core is fed to a nonlinear limiting amplifier with a load resonant at $3f_0$. This technique, however, suffers from low f_0 to $3f_0$ efficiency of the limiting amplifier at mm-wave, and has a significant tradeoff between the output power at $3f_0$ and the dc power consumption of the nonlinear limiting amplifier. Fig. 2(c) presents an injection-locked frequency multiplier (ILFM) concept where the frequency of the mm-wave VCO is locked by using an auxiliary oscillator operating at a lower frequency [11]–[13]. Due to the noise-shaping of the locked oscillator, the output ILFM signal has a superior PN performance than a free-running oscillator [11]. However, design considerations like power consumption, complexity, and injection locking-range must be addressed for ILFM. The injected subharmonic signal should be strong enough to lock the output to the desired frequency, necessitating power hungry amplification stages. For example, designs in [12] and [13] consume significant power in gain stages, buffer, and injection-locking oscillator (ILO). Designing mm-wave buffers and calibration for ILO adds to the design complexity ([13], Table I). The FTR of the ILO is usually limited by the locking-range. To the best of our knowledge, the typical locking-range of mm-wave ILOs is in the range of 7%–14%.

Although several designs for indirect and direct synthesis are presented in literature, the approach resulting in a superior performance still remains a matter of debate [4]. In this paper, after discussing the benefits of H-VCO versus F-VCO, we present a self-mixing VCO (SMV), whose basic topology is shown in Fig. 2(d) [14]. Instead of generating a $3f_0$ component out of the VCO, the SMV utilizes the second harmonic ($2f_0$) from the common-mode output along with the fundamental (f_0) from the differential output—we refer to this VCO as a 3H-VCO from now on. The amplitude of $2f_0$ signal that can be extracted from a VCO is larger than the amplitude of $3f_0$ signal, thereby making it a superior implementation than [3]. Furthermore, the SMV architecture does not suffer from strict matching requirements, single-ended operation, and large power consumption of the triple push VCO [3]. Finally, we propose the use of a Class-C VCO topology to further enhance the amplitude of the $2f_0$ component and improve the PN. Thus,

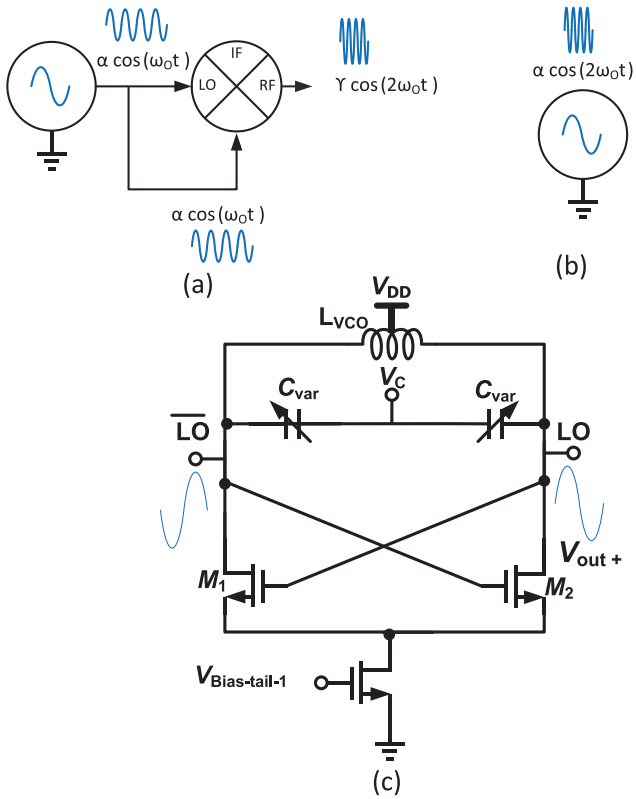

Fig. 3. (a) 2H-VCO and (b) F-VCO, both generating $2\omega_0$. (c) Conventional Class-B VCO core.

the specifications for a low PN, large tuning range, and low dc power can be simultaneously met.

This paper is organized as follows. Section II compares direct and indirect signal generation with focus on the PN performance. Section III describes the proposed Class-C SMV architecture in details. Section IV presents the measurement results of a proof-of-concept prototype SMV that is implemented in a 0.13 μm CMOS as well as performance comparison with the state-of-the-art designs. Section V provides concluding remarks.

II. PN and FoM Comparison of Direct and Indirect Signal Synthesis

Consider a 2H-VCO and an F-VCO, both generating $2\omega_0$, as shown in Fig. 3(a) and (b), respectively. The core oscillator in 2H-VCO operates at ω_0 and uses an upconverter (e.g., mixer) to achieve $2\omega_0$, with the PN of the final output at $2\omega_0$ about $20\log(2)$ higher than that of the core oscillator, assuming the up-conversion process to add negligible AM to PM noise. Based on Hajimiri's PN theory [15], it can be shown that the PN of the F-VCO is larger than the overall PN of the 2H-VCO, with the excess PN given by

$$\mathrm{PN}_{\mathrm{excess}} = 10\log\left(\frac{R_{T,2\omega_0}}{R_{T,\omega_0}}\cdot\left(\frac{A_{\omega_0}}{A_{2\omega_0}}\right)^2 \cdot\frac{{\Gamma_{T,\mathrm{rms},2\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms}-eff,2\omega_0}}^2}{{\Gamma_{T,\mathrm{rms},\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms}-eff,\omega_0}}^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right) \quad (1)$$

where R_T represents the tank parallel loss, A is the oscillation amplitude, $\Gamma_{T,\mathrm{rms}}$ is the rms values for impulse sensitivity function (ISF) of R_T noise, $\Gamma_{M,\mathrm{rms\text{-}eff}}$ is the rms value for the effective ISF of transistor [M_1 or M_2 shown in the conventional Class-B oscillator of Fig. 3(c)] thermal noise, and γ is the excess noise factor of a MOS transistor [15]. The subscripts ω_0 and $2\omega_0$ in (1) are associated with the 2H-VCO and F-VCO, whose cores are operating at these frequencies, respectively.

Different oscillators are compared in terms of an FoM that normalizes the phase noise (PN) to the oscillation frequency, the offset frequency, and the power dissipation (expressed in mW or dBm) [14]; considering the VCO FoM $=$ PN $+$ $10\log(P_{\mathrm{dc,mW}}\cdot\left(\frac{\Delta f}{fo}\right)^2)$, $\mathrm{FoM}_{\mathrm{excess}}$ can be defined as

$$\mathrm{FoM}_{\mathrm{excess}} = \mathrm{FOM}_{\mathrm{HVCO}} - \mathrm{FOM}_{\mathrm{FVCO}} \approx \mathrm{PN}_{\mathrm{excess}}(Q,\Gamma,N) + 10\log\left(\frac{P_{\text{dc-FVCO}}}{P_{\text{dc-HVCO}}}\right). \quad (2)$$

Defining the tank dissipated RF power as $P_{\mathrm{RF}} = \frac{A^2}{R_T} = I_{\mathrm{RF,rms}}.V_{\mathrm{RF,rms}}$ and $P_{\mathrm{dc}} = I_{\mathrm{dc}}.V_{\mathrm{dc}}$, (2) can be simplified for a 2H-VCO as

$$\mathrm{FoM}_{\mathrm{excess}} = 10\log\left(\left(\frac{\eta_{V,\omega_0}.\eta_{I,\omega_0}}{\eta_{V,2\omega_0}.\eta_{I,2\omega_0}}\right)\cdot\left(\frac{{\Gamma_{T,rms,2\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms\text{-}eff},2\omega_0}}^2}{{\Gamma_{T,rms,\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms\text{-}eff},\omega_0}}^2}\right)\cdot\left(\frac{Q_{\omega_0}}{Q_{2\omega_0}}\right)^2\right) \quad (3)$$

where η_V and η_I are voltage and current efficiencies [19], respectively. For an NH-VCO with an up-conversion ratio of N and output frequency of $N\omega_0$, (2) can be generalized as

$$\mathrm{FoM}_{\mathrm{excess}}(Q,\Gamma,N) = 10\log\left(\left(\frac{\eta_{V,\omega_0}.\eta_{I,\omega_0}}{\eta_{V,N\omega_0}.\eta_{I,N\omega_0}}\right)\cdot\left(\frac{{\Gamma_{T,rms,N\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms\text{-}eff},N\omega_0}}^2}{{\Gamma_{T,rms,\omega_0}}^2+\gamma{\Gamma_{M,\mathrm{rms\text{-}eff},\omega_0}}^2}\right)\cdot\left(\frac{Q_{\omega_0}}{Q_{N\omega_0}}\right)^2\right). \quad (4)$$

Equation (4) reveals dependency of $\mathrm{FoM}_{\mathrm{excess}}$ to Q, ISF, and the device efficiency (e.g., current and voltage efficiencies). Although at lower frequencies, Q for the two VCOs can be almost the same, as we approach mm-wave region the difference in Q for the two oscillators becomes higher and thus HVCO can show a better PN and FoM than FVCO (by every doubling Q, FoM improves by about 6 dB). Second, as will be discussed, ISFs of both active and passive devices are predicted to be higher in mm-wave range. In addition to ISF and Q degradation, device efficiency (e.g., transconductance efficiency and power gain) decreases as the oscillation frequency approaches the maximum oscillation frequency ($f_{\max}$) of the transistors. Hence, an excess power is required to guarantee a sustained oscillation which in turn impacts FoM.

Here, we simplify (4) for two different cases. First, assuming that both cores of NH-VCO and F-VCO generate the same signal swing ($\eta_{V,\omega_0} = \eta_{V,N\omega_0}$), (it should be noted that assuming $A_{\omega_0} = A_{N\omega_0}$ potentially results in a higher current consumption in the F-VCO mainly due to lower passive quality factors

as well as degradation of the device efficiency). With this assumption, $\text{FOM}_{\text{excess}}$ can be simplified as

$$\text{FoM}_{\text{excess}}(Q,\Gamma) = 10\log\left(\left(\frac{\eta_{I,\omega_0}}{\eta_{I,N\omega_0}}\right)\frac{\Gamma_{T,\text{rms},N\omega_0}{}^2+\gamma\Gamma_{M,\text{rms-eff},N\omega_0}{}^2}{\Gamma_{T,\text{rms},\omega_0}{}^2+\gamma\Gamma_{M,\text{rms-eff},\omega_0}{}^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{N\omega_0}}\right)^2\right). \quad (5)$$

Second, assume that both cores of NH-VCO and F-VCO consume same power $(I_{\text{dc-}\omega_0} = I_{\text{dc-}N\omega_0}), \approx \eta_I I_{\text{dc}} R_T$, and assuming R_T be proportional to Q (e.g., $R_T = LQ\omega_0$), and L is chosen to be inversely proportional to ω_0, $\text{FOM}_{\text{excess}}$ can be simplified as

$$\text{FoM}_{\text{excess}}(Q,\Gamma) = 10\log\left(\left(\frac{\eta_{I,\omega_0}}{\eta_{I,N\omega_0}}\right)^2\frac{\Gamma_{T,\text{rms},N\omega_0}{}^2+\gamma\Gamma_{M,\text{rms-eff},N\omega_0}{}^2}{\Gamma_{T,\text{rms},\omega_0}{}^2+\gamma\Gamma_{M,\text{rms-eff},\omega_0}{}^2}\cdot\left(\frac{Q_{\omega_0}}{Q_{N\omega_0}}\right)^3\right). \quad (6)$$

The following sections analyze and compare the ISF and Q of the two VCO topologies to estimate $\text{PN}_{\text{excess}}$ (or equally $\text{FoM}_{\text{excess}}$), and therefore, the low PN merits of H-VCOs.

A. Comparison of On-Chip Passives

The quality factor of a mm-wave LC-tank can be limited by either quality factor of the inductor, namely Q_L, or quality factor of the capacitor and varactor, namely Q_C. The design of the tank must be carried out with two considerations—operating at the maximum achievable Q which minimizes PN and power consumption, and, using $f_{\text{osc}} = \frac{1}{2\pi\sqrt{LC}}$, the inductance should be sufficiently small so that the tank requires additional explicit capacitance provided by the varactor to maximize the FTR of the VCO.

Generally, Q_L of a spiral inductor is limited by loss in the metal lines and the substrate, which at mm-wave frequencies is frequency dependent due to factors such as skin effect and proximity effect [16]. Using a double-π equivalent model [17] for inductors, it can be shown that at low frequencies, Q_L increases with frequency until it reaches its maximum value $Q_{\max}$, beyond which it drops, as the frequency-dependent loss becomes significant. One way to reduce the substrate-loss and increase Q_L in mm-wave range is to reduce the effective substrate area under the inductor by decreasing the width [16], and the number of turns of the inductor. In this paper, Q_L of a single-turn octagonal inductor, suitable for mm-wave signal generation, is studied. The structure is shown in Fig. 4. The inductance is adjusted by changing the radius and the width of the metal layer. For the purpose of simulation, both *Sonnet* and *PickView* 3-D planar EM simulators are used. Fig. 4 presents differential inductance, maximum achievable differential quality factor, $Q_{\text{diff-max}}$, and the frequency at which Q_L reaches its maximum value, namely $f_{Q\text{-max}}$, versus the octagonal radius (R) for three different metal widths $(W = 40, 10, \text{ and } 4\ \mu\text{m})$. For a 3H-VCO with its core oscillator operating at 20 GHz, a high $Q_{\text{diff-max}} \approx 36$ at 20 GHz is obtained with 175 pH of

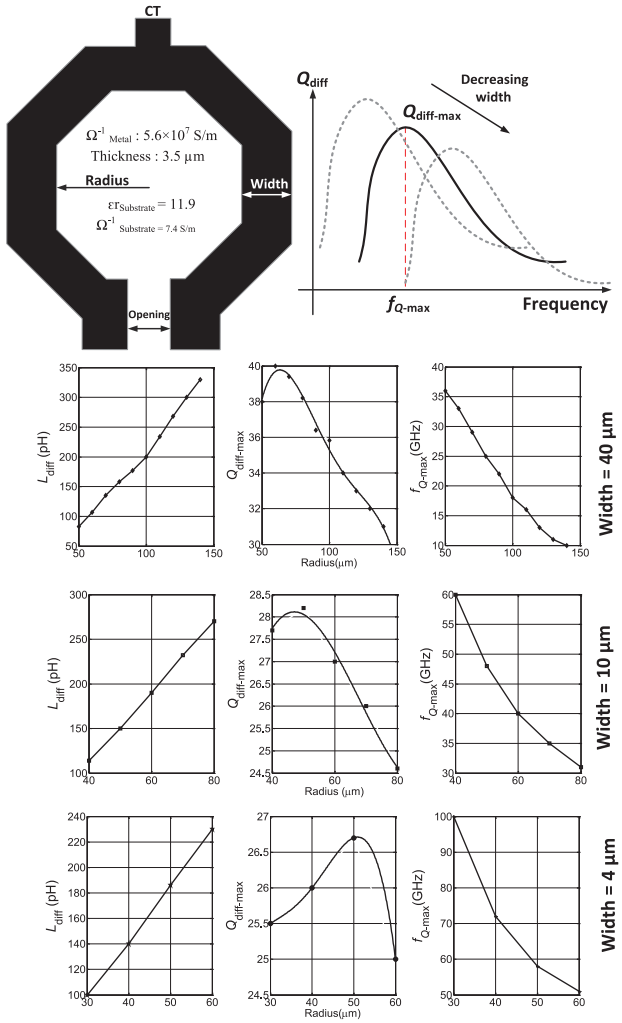

Fig. 4. Differential inductance (L_{diff}), maximum differential quality factor ($Q_{\text{diff-max}}$), and the frequency where the quality factor reaches its maximum value ($f_{Q\text{-max}}$) versus radius (R) of inductor for three different inductor widths.

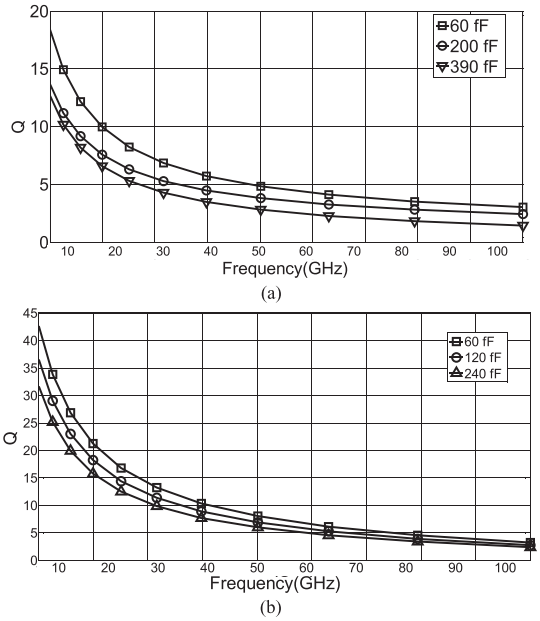

Fig. 5. Quality factor of (a) MOS varactors with 30% tuning range and (b) mimcaps.

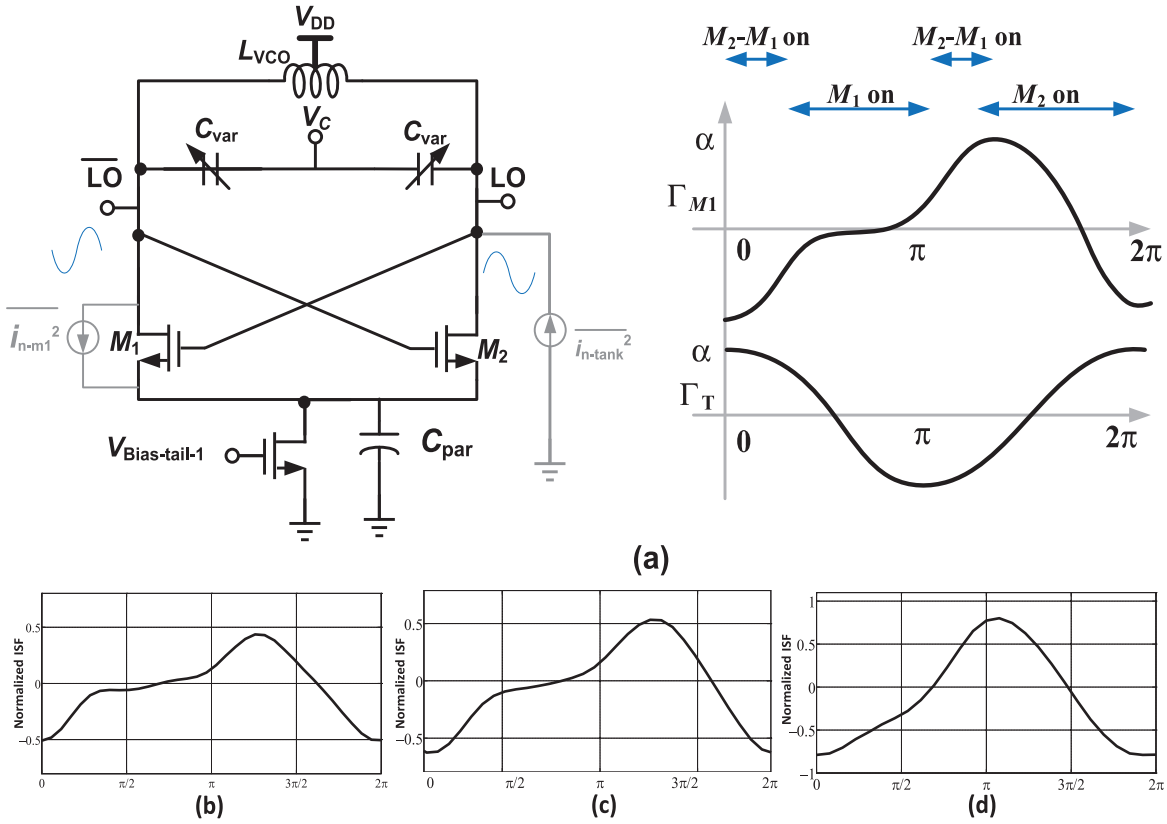

Fig. 6. (a) Conceptual ISFs, Γ_M, and Γ_T at low frequency for a Class-B VCO. Simulated Γ_M at (b) 7GHz, (c) 21 GHz, and (d) 63 GHz, respectively. ISF is normalized to the maximum charge displacement, q_{max} [15].

inductance ($W = 40$ μm, $R = 95$ μm), yielding about 350 fF of tank capacitance. On the other hand, for an F-VCO operating at 60 GHz, an inductor having a $Q_{\text{diff-max}}$ at 60 GHz for best PN performance limits FTR by permitting small tank capacitance (W=10 μm, R=40 μm, $Q_{\text{diff-max}}$=27.9, L=120 pH, C=55 fF; or $W = 4$ μm, $R = 48$ μm, $Q_{\text{diff-max}}$=26.6, $L = 180$ pH, $C =$ 38 fF), or a lower $Q_{\text{diff-max}}$ of 19.1−19.7 for larger FTR through the choice of smaller inductance (40−60 pH) for $W = 10$ μm. If the inductor limits the quality factor of the LC-tank, (3) suggests that the 3H-VCO could have $10\log\left(\frac{Q_{\text{3H-VCO}}}{Q_{\text{F-VCO}}}\right) \approx 2.7$ dB better PN. As Q_{tank} is dictated by the loss in inductors as well as in MOS varactors and the metal-insulator-metal capacitors (mimcaps) at the mm-wave range of operation ($\frac{1}{Q_{\text{tank}}} \approx \frac{1}{Q_L} + \frac{1}{Q_{\text{mimcap}}} + \frac{1}{Q_{\text{moscap}}}$), the overall Q_{tank} may be dominated by the varactor loss, which often shows a lower Q due to the use of lower metal layer connections to the MOS device. Fig. 5 show how the Q of the MOS-varactor and mimcap degrades with frequency, for three different capacitor values. Q_{tank} for this technology is clearly limited by the loss in the MOS varactors. Clearly, a 3H-VCO operating at 20 GHz core can achieve significantly higher Q_{tank} than that of an F-VCO operating at 60 GHz.

B. Comparison of ISF in A Class-B VCO

Next, we analyze the effect of increasing the operating frequency of the VCO core on $\Gamma_{M,\text{rms-eff}}$ and $\Gamma_{T,\text{rms}}$. Consider a conventional Class-B oscillator and its associated Γ_M and

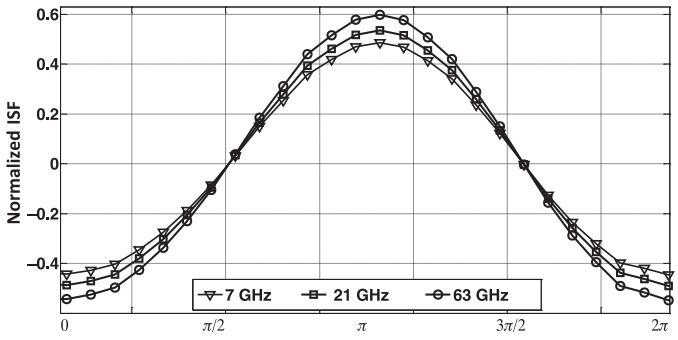

Fig. 7. Simulated Γ_T of a Class-B VCO at 7, 21, and 63 GHz (single-ended noise is injected). ISF is normalized to the maximum charge displacement q_{max} [15].

Γ_T as shown in Fig. 6(a). A detailed study of Class-B topology can be found in [18]. First, let us consider the ISF for M_1, namely Γ_M. Based on the operating region of transistors (deep triode or cut-off), the current noise of M_1 finds two major paths to reach the output node and generate PN—through M_2 when M_2 turns ON, or through the parasitic tail capacitance C_{par} via the ground when M_2 is OFF and M_1 is ON. At low operating frequency, the impedance of C_{par} is negligible, and the noise current only reaches the output when the switches are commutating, through M_2. This results in almost a flat zero area in Γ_M when M_2 is OFF. However, as frequency increases, the effect of C_{par} becomes more significant and $\Gamma_{M1,\text{rms}}$ increases, as seen in the plots for Γ_M at 7, 21, and 63 GHz (all simulations

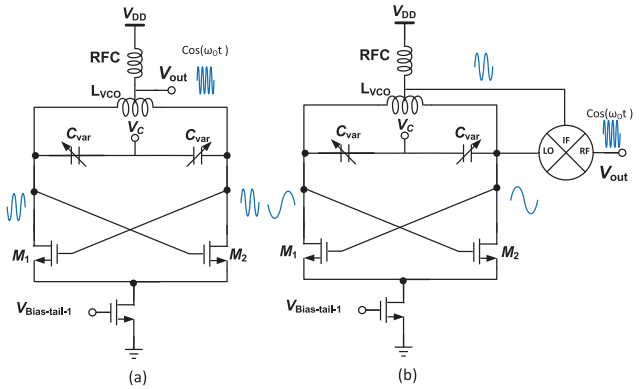

Fig. 8. (a) 2H-VCO (push–push Class-B core). (b) 3H-VCO with SMV architecture (Class-B core).

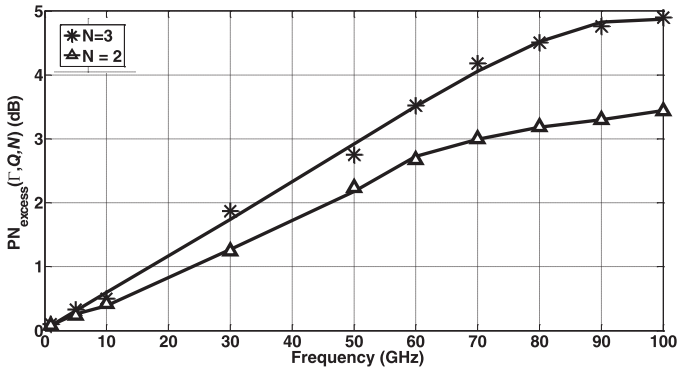

Fig. 9. Simulation results for $\mathrm{PN}_{\mathrm{excess}}$ for $N = 2$ and 3. PN is simulated at 1 MHz offset frequency.

have been done with the same Q_{tank} and core transistors are optimized to reach the lowest PN) in Fig. 6(b)–(d), respectively. Two conclusions can be easily made here. 1) Due to the lower core frequency, H-VCO architecture has smaller $\Gamma_{M,\mathrm{rms\text{-}eff}}$ than F-VCO, thereby providing a better PN. 2) To alleviate the effect of C_{par} in mm-wave range, one can use an alternative topology which has less sensitivity to the tail parasitic capacitance. For example, a Class-C VCO topology can be attractive in which the transistors are operating in saturation region and are ON for only for a small amount of time (typically around the peak of the output voltage), and thus the effective injected noise and ISF of the core transistors can be reduced. In this case, a larger tail capacitance should be used to facilitate a proper operation of class-C, filtering the high frequency noise of the tail transistor. In addition to noise filtering, class-C operation provides a superior current efficiency η_I [19].

As for the tank-referred ISF $\Gamma_{T,\mathrm{rms}}$, it is expected that $\Gamma_{T,\mathrm{rms}}$ increases when operating at the mm-wave range. This is predominantly due to increased AM to PM noise conversion from the nonlinear capacitances of active core transistors which have comparable size to varactors at the higher frequency. Fig. 7 shows the simulation results of $\Gamma_{T,\mathrm{rms}}$ versus frequency (all simulations have been done with the same Q_{tank} and core transistors, while the frequency is changed by adjusting the value of the tank capacitance. Single-ended noise is injected and all plots are normalized to the maximum charge displacement $\mathrm{q}_{\mathrm{max}}$ [6], [15]). As shown, increasing the frequency from 20 to 60 GHz increases $\Gamma_{T,\mathrm{rms}}$ by about 26.8%.

C. PN_{excess} of a Class-B VCO for Different Up-Conversion Ratios

In the previous section, we compared and discussed the parameters which are contained in $\mathrm{PN}_{\mathrm{excess}}(Q, \Gamma, N)$. To have a better understanding of realistic values for $\mathrm{PN}_{\mathrm{excess}}\ (Q, \Gamma, N)$, a 2H-VCO and 3H-VCO are compared with an F-VCO at different frequencies. Here, the F-VCO is realized with a Class-B oscillator [Fig. 3(c)], 2H-VCO is implemented using a push–push Class-B VCO [Fig. 8(a)], and the 3H-VCO is achieved by self-mixing the output of a Class-B and the second harmonic from the tail using an ideal mixer [Fig. 8(b)]. In each simulation, the LC-tank and the active-cores are separately optimized for the target frequency to achieve the minimum PN (all inductors are designed and optimized using PickView). Fig. 9 presents the simulation results of $\mathrm{PN}_{\mathrm{excess}}\ (Q, \Gamma, 3)$ and $\mathrm{PN}_{\mathrm{excess}}\ (Q, \Gamma, 2)$ for a 1–100 GHz oscillator. As predicted, at low frequencies (e.g., less than 10 GHz) where the quality factor of passives and ISFs of H-VCO and F-VCO are close to each other, $\mathrm{PN}_{\mathrm{excess}}$ is negligible. However, as the frequency increases, H-VCO shows a better PN performance due to the superior Q and noise sensitivity of the core oscillator. In the next section, we discuss the implementation of the proposed 3H-VCO.

III. Proposed 60 GHz 3H-VCO

As suggested earlier, Class-C operation can alleviate the detrimental effect of tail parasitic capacitance in increasing $\Gamma_{M,\mathrm{rms}}$ by changing the operating region of the transistors. We will further show that a Class-C topology can also provide a lower active-core parasitic capacitance across the LC-tank and hence an improved FTR. Thus, we focus our attention on the Class-C implementation in this section.

Fig. 10 illustrates two possible architectures for achieving a Class-C 3H-VCO. In Fig. 10(a), the third harmonic of a Class-C oscillator is extracted using a tuned transformer at 60 GHz. An alternative SMV is shown in Fig. 10(b). In the first stage, the structure uses a Class-C push–push VCO to generate f_0 and $2f_0$ components at 20 and 40 GHz, respectively. In the second stage, a single-balanced active mixer is used to combine the f_0 and $2f_0$ components and generate the desired LO component at $3f_0(\sim 60\ \mathrm{GHz})$ at the output of the mixer. A $\lambda/4$ (at $2f_0$) transmission-line is used for biasing the VCO and mixer as well as to maximize the second-harmonic component. This $\lambda/4$ line is ideally open (high impedance) at $2f_0$ and allows the second harmonic current $I_2 f_0$ to sink into the mixer. The mixer is tuned at $3f_0(\sim 60\ \mathrm{GHz})$ to provide frequency selectivity and suppress spurious components at the lower mixing sideband. To avoid a transformer design, and the adverse effect it has on the Q of the core tank that oscillates at the fundamental frequency degrading the PN and FoM, in this work, we focus on implementation of the Class-C SMV as shown in Fig. 10(b).

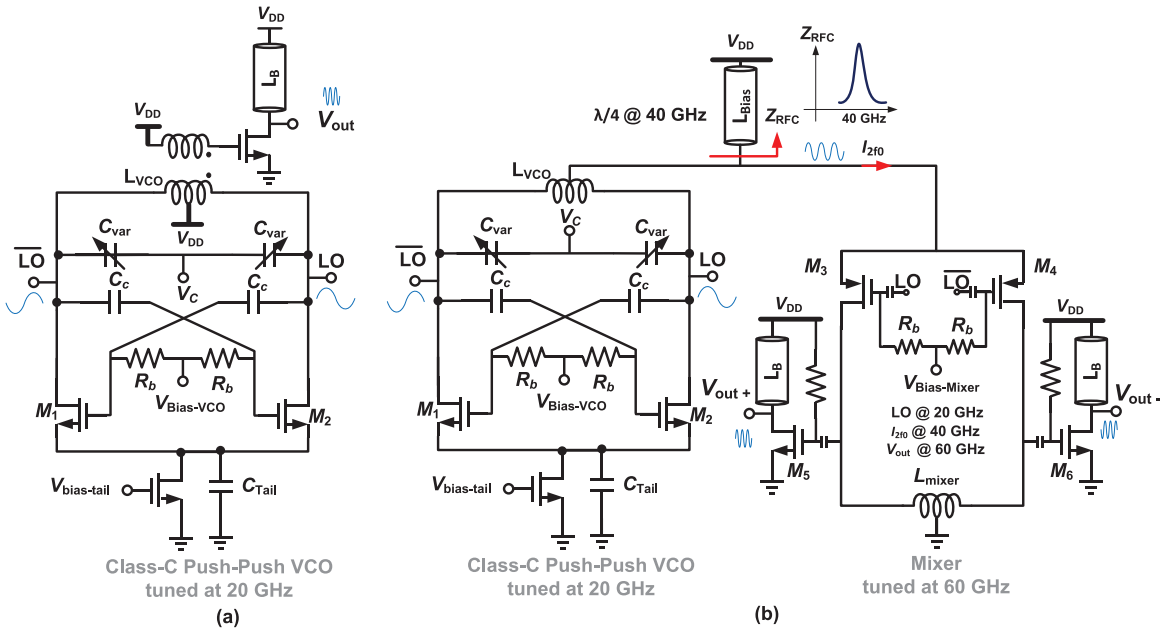

Fig. 10. (a) Transformer-based third harmonic extraction. (b) SMV implementation [14].

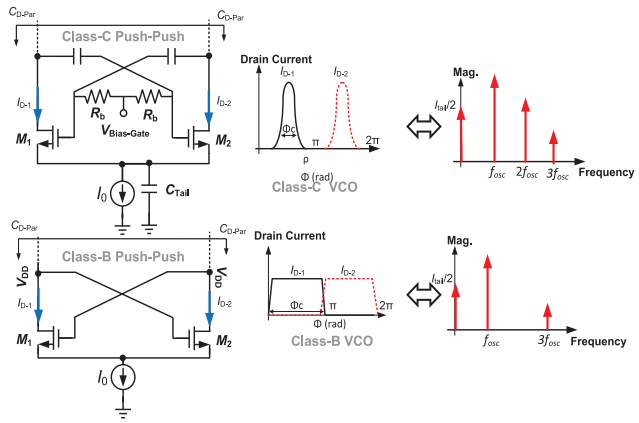

Fig. 11. Cross-coupled pair in Class-C and Class-B VCOs and corresponding drain currents.

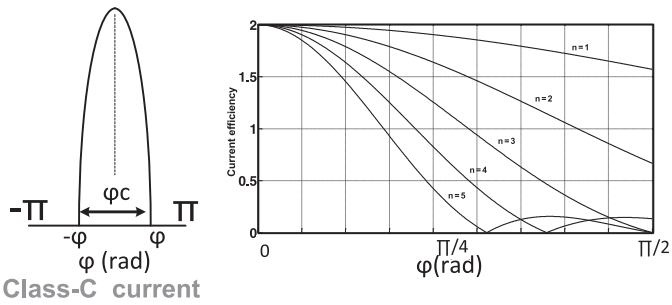

Fig. 12. Current efficiency versus conduction angle.

TABLE I
OPERATING REGION OF TRANSISTORS IN CLASS-B VCO

Operating region	C_{core}
I. Small swing M_1 & M_2 in saturation	$C_{gs1} + 4C_{gd1} + 4C_{db1} \approx \frac{2}{3}WLC_{\text{ox}} + 5WC_{\text{ov}}$
II. (or IV) medium swing M_1 off, M_2 in saturation or vice-versa	$\frac{-1}{2}\frac{{g_m}^2 C_{\text{Tail}}}{{g_m}^2 + (C_{\text{Tail}} + C_{gs})^2\omega^2} + 4C_{gd1}$
III. Large swing M_1 off, M_2 in triode	$\frac{1}{2}\frac{{g_{ds}}^2.(2C_{gs} + C_{\text{Tail}})}{{g_{ds}}^2 + (C_{\text{Tail}} + C_{gs})^2\omega^2} + 2C_{gd1} + \frac{C_{db}}{2}$

A. *Benefits of Using Class-C Push–Push VCO in mm-Wave*

The operational Class of core VCO significantly impacts the amount of $2f_0$ component generated at its output. A smaller $2f_0$ component reduces the conversion gain of the mixer in SMV, thereby necessitating a larger power consumption in the mixer to increase the signal swing of the $3f_0$ output signal. The Class-B push–push VCO has been frequently used for generating $2f_0$ [20], [21]. However, it achieves low dc-to-$2f_0$ efficiency due to the nature of the VCO current waveforms. Fig. 11 shows a Class-B cross-coupled VCO, where the cross-coupled transistors (M_1 and M_2) operate mostly in triode region. In contrast, in a Class-C design, with $V_{\text{Bias-Gate}} < V_{\text{DD}}$, these transistors operate in the saturation region when conducting. Also, a Class-C VCO employs a large capacitor in parallel to the tail device. In comparison to the ideal Class-B operation with square-wave drain current, Class-C VCO shows a (Class-C) waveform with conduction angle of $\Phi_C < \pi$ [22]. This has two main benefits: first, while the square-wave drain current has a zero second-order harmonic in ideal Class-B operation (although in a real implementation, the current waveform is not an ideal square-waveform and does contain some second harmonic), the Class-C drain-current results in generating a larger first and second harmonic and consequently higher dc-to-f_0 and dc-to-$2f_0$ efficiencies. An expression for the dc-to-nf_0 current efficiency ($\eta_{I,n}$) for the Class-C operation is derived later in the Appendix, and is plotted in Fig. 12 as a function of one-half the conduction angle for various n. The second benefit of Class-C, as shown in [18], [22] and attributed to its better current efficiency, is that Class-C drain current waveform in VCOs results in 3.9 dB lower PN at same dc power consumption (or 50% lower dc current while achieving the same PN [22]).

In addition to a better dc-to-$2f_0$ efficiency and superior PN performance, the Class-C VCO has a lower parasitic capacitance C_{core} across the resonator LC-tank.

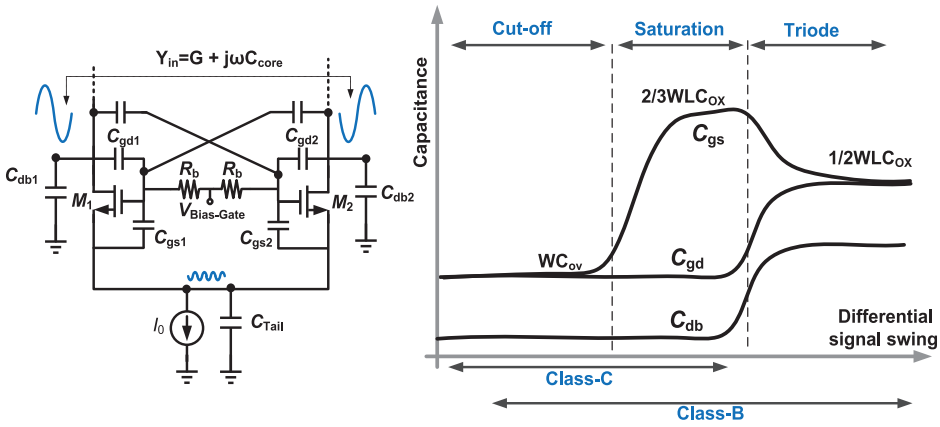

Fig. 13. Parasitic capacitances in a cross-coupled oscillator.

TABLE II
OPERATING REGION OF TRANSISTORS IN CLASS-C VCO

Operating region	C_{core}
I. Both M_1 & M_2 off	$\approx 4C_{\text{gd,off}} + C_{\text{gs1,off}} = 5\text{W}C_{\text{ov}}$
II. (or III.) M_1 off, M_2 in saturation or vice-versa	$\approx C_{\text{gs}}$

Consider a cross-coupled pair and its associated parasitics as shown in Fig. 13. Here, C_{core} presents the amount of the active core parasitics and is a function of $C_{gs}, C_{gd}, C_{db}, g_m, g_{ds}$, and C_{Tail}. As shown in [23], transistors in a class B core undergo four different operating regions over a complete period of signal swing. Table I shows the different operating regions, and the expression for instantaneous C_{core} in each region [23]. Here, C_{ov} is the overlap capacitance per unit channel width (W), and C_{OX} is the gate oxide capacitance per unit area. $\frac{1}{\sqrt{LC}}$

From Table I and Fig. 13, even though C_{gs} is larger or equal to C_{gd} in all the operating regions, the effect of C_{gd} in C_{core} is amplified by $4\times$ due to differential swings and is dominant. In operating region III, both C_{gd} and C_{db} are large, and if C_{Tail} is designed in Class-B operation to be large in order to reduce the flicker noise upconversion at the output PN, C_{core} becomes significantly large in this region. Averaging over the entire period, the large signal parasitic capacitance $(C_{D\text{-par}})$ for Class-B remains considerably big, severely limiting the tuning range at mm-wave frequencies.

On the other hand, in order to find the instantaneous small-signal capacitance of a class-C VCO, the oscillation period can be divided in three regions: 1) when both cross-coupled transistors are OFF and 2) [or 3)] when only one device is ON and operates in the saturation region. Table II shows the different operating regions in a Class-C operation, and the expression for instantaneous C_{core} in each region. By avoiding operating in triode region, and with a conduction angle smaller than Class-B, a Class-C core therefore has much lower $C_{D\text{-par}}$, and, therefore, a larger tuning range at mm-wave frequencies.

To validate the above-mentioned analysis, $C_{D\text{-Par}}$ for a Class-C and Class-B VCOs is simulated. To have a fair comparison and observe only the effect of the operation region on $C_{D\text{-Par}}$, identical core transistors and current sources are used. The parasitic capacitance of the current source is about 200 fF. For the

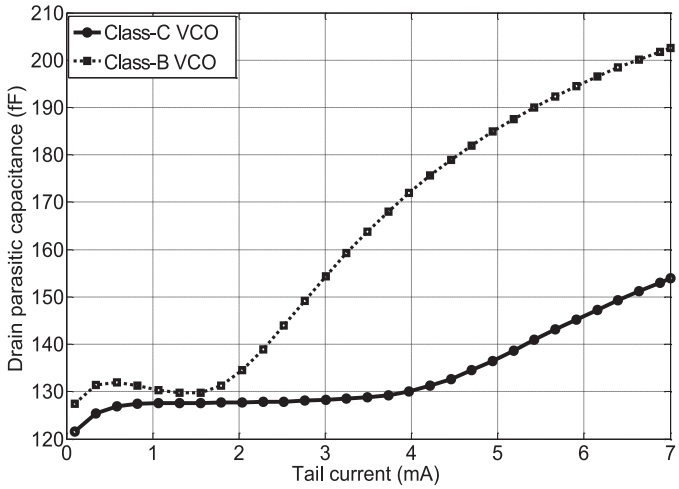

Fig. 14. Parasitic capacitance $(C_{D-\text{Par}})$ of cross-coupled pair in Class-B and Class-C VCO at 20 GHz.

Class-C design, a 1 pF capacitance is added at tail (C_{tail}) to ensure a proper Class-C operation. Fig. 14 compares the simulated drain capacitance. As can be seen, $C_{D\text{-Par}}$ in Class-C is almost 2/3 of that of Class-B. A Class-C VCO therefore ensures a higher FTR, especially at mm-wave frequencies.

B. Comparison of Output Signal Swing

VCOs are often designed and compared in terms of PN, FTR, and power dissipation. Two popular figures of merit (FoMs) for comparing VCOs are

$$\text{FOM} = \text{PN} - 20\log(fo/\Delta f) + 10\log(P_{\text{dc}}/1\text{ mW}) \quad (7)$$

$$\text{FOM}_T = \text{FOM} - 20\log(FTR/10). \quad (8)$$

Although these FoMs are applicable to mm-wave VCOs, and indeed widely used and reported [1], [3] they do not directly incorporate the output signal swing of the VCOs or the power consumption of the buffers. The buffers are often designed to be able to drive 50 Ω for test purposes, *including* the prototype presented in Section IV.

In order to use a mm-wave VCO in a monolithic transceiver, it must have a significantly high voltage swing and be able

TABLE III
SIMULATED PERFORMANCE COMPARISON OF 60 GHZ VCO TOPOLOGIES

Parameters	Active-mixer 3H-VCO	Passive-mixer 3H-VCO	Active-mixer 2H-VCO	Passive-mixer 2H-VCO	F-VCO
Mixer gain (V/A Ohm) *	**152.46**	**28.60**	**150**	**28.52**	**NA**
PN (dBc/Hz) @ 1 MHz	–102.4	–101.5	–97.2	–96.8	–94.7
FTR %	10.3	10	8.3	5.8	4.0
Single-ended voltage Swing (mV_{pk-pk})	900	900	900	900	900
Power (core) (mW)	18.5	17.4	21.4	16.2	16.36
Power (buffer) (mW)	10.3	25.8	10.4	11.2	4.28
Total power (mW)	28.8	43.2	31.4	24.4	20.64
FoM (dBc/Hz) (core) @ 60 GHz	–185.3	–184.6	–179.43	–180.26	–178.13
FoM (dBc/Hz) (core+buffer)	–183.36	–180.7	–177.77	–178.08	–177.12
FoM_T (dBc/Hz) (core+buffer)	–183.62	–180.7	–176.15	–173.04	–169.16

*Since the mixers are operating in current mode, fed by the harmonic current generated by the push-push VCO at the VCO common-mode node, the gain of the mixer is in Ohm.

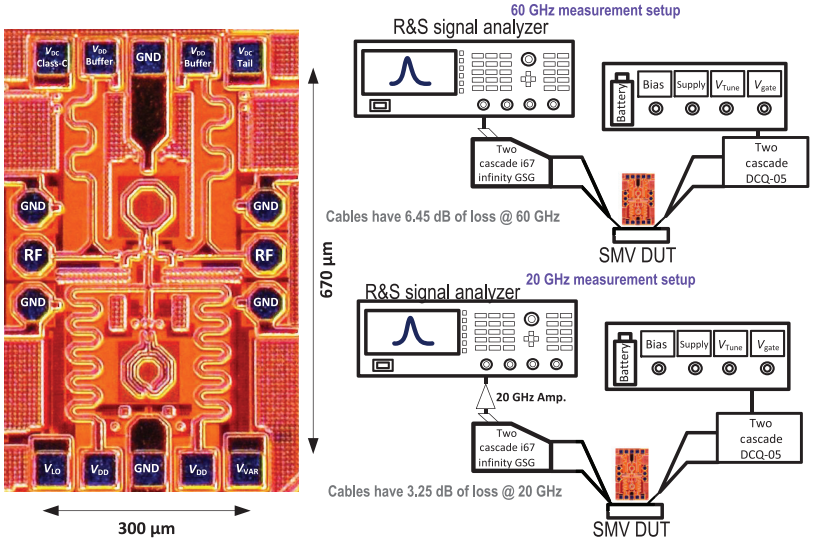

Fig. 15. Measurement setup and chip micrograph of SMV architecture.

to drive a capacitive load. F-VCOs usually have large signal swings, although at the expense of a severe tradeoff with FTR, PN, and power dissipation to start and ensure oscillations. On the other hand, H-VCOs have improved PN, FTR, and power dissipation in the core as described earlier, but suffer from insufficient output swing. In order to amplify the signal swing, additional power must be consumed in buffers that can drive a capacitive load.

For a fair comparison between F-VCO and H-VCOs for the case of similar output signal swing, five different topologies are simulated, as shown in Table III. This includes a 60 GHz F-VCO, a 60 GHz 2H-VCO [Fig. 3(a)] with the core operating at 30 GHz, and a 60 GHz 3H-VCO [Fig. 10(b)] with the core operating at 20 GHz. All the cores use a Class-C topology for fair comparison in terms of FTR and PN. For the H-VCOs, the output of the mixer is amplified using a three-stage buffer, each stage being a common-source buffer with a 1:2 transformer-based resonant load at 60 GHz. The final stage drives a 30 fF load with a single ended swing of at least 900 mV, assumed to be sufficiently large to switch transistors ON/OFF in 130 nm CMOS process. The 1:2 transformers in the buffer are implemented with a quality factor of 10 in the primary and secondary turns. For the F-VCO, only one stage of

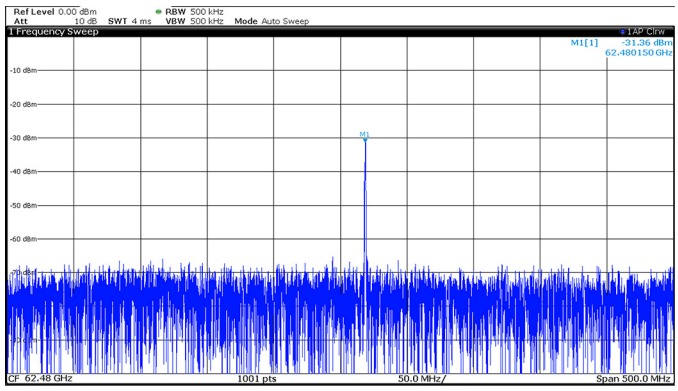

Fig. 16. Measured SMV spectrum at the buffer output at 62.48 GHz.

buffer is needed. Furthermore, for each H-VCOs, both active [Fig. 10(b)] and passive mixers are implemented. The main concerns for the mixer design are the capacitive loading for the core and the conversion gain, which are best addressed by an active mixer. However, passive mixers, implemented using transmission gates, as presented in [16], do not consume static power. The common-mode input levels of the passive mixer are held to ground to reduce power consumption. No considerable

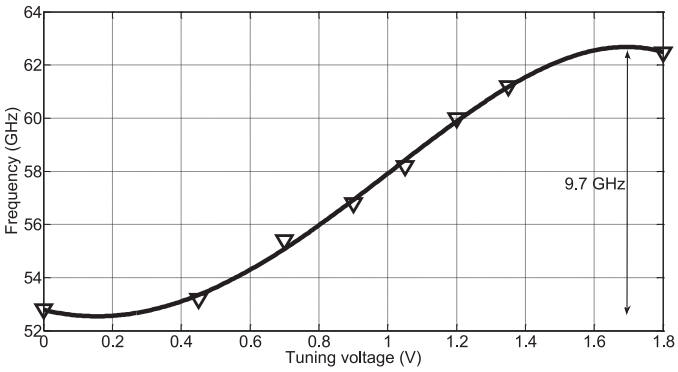

Fig. 17. Measured frequency tuning range.

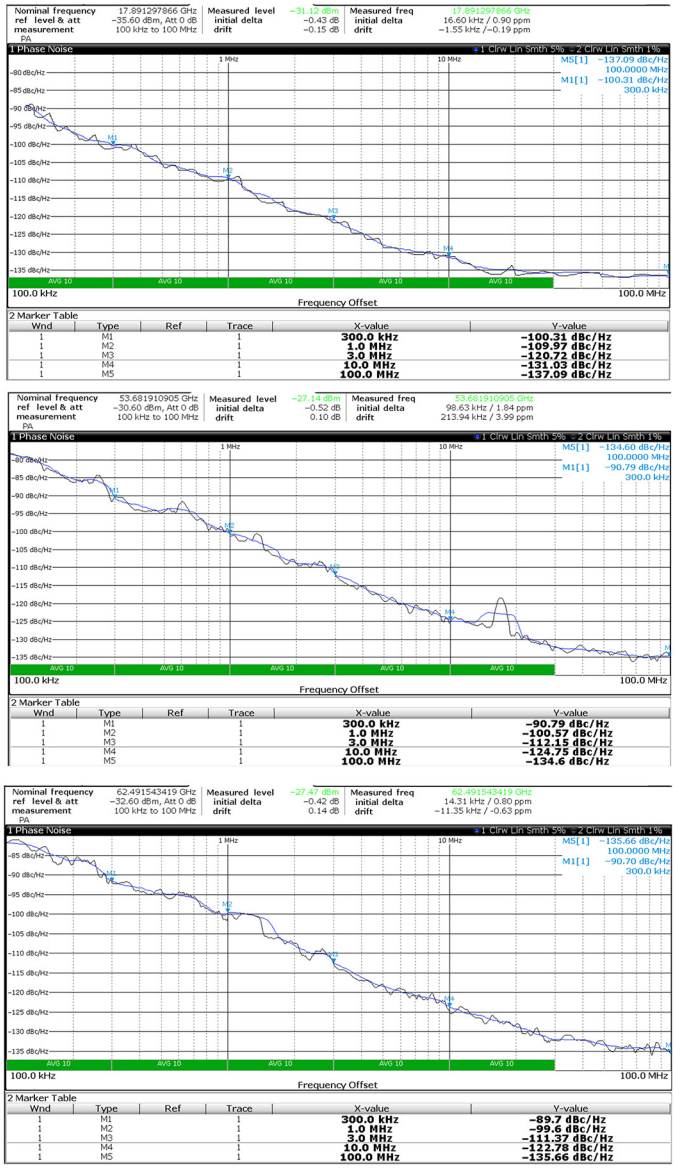

Fig. 18. Measured SMV phase noise at 17.9 GHz (fundamental), 53.68 GHz (tripled, lowest frequency), and 62.49 GHz (tripled, highest frequency).

PN performance difference in passive versus active mixer is seen for the same H-VCO design. Each of the designs is operated at 1.2 V supply.

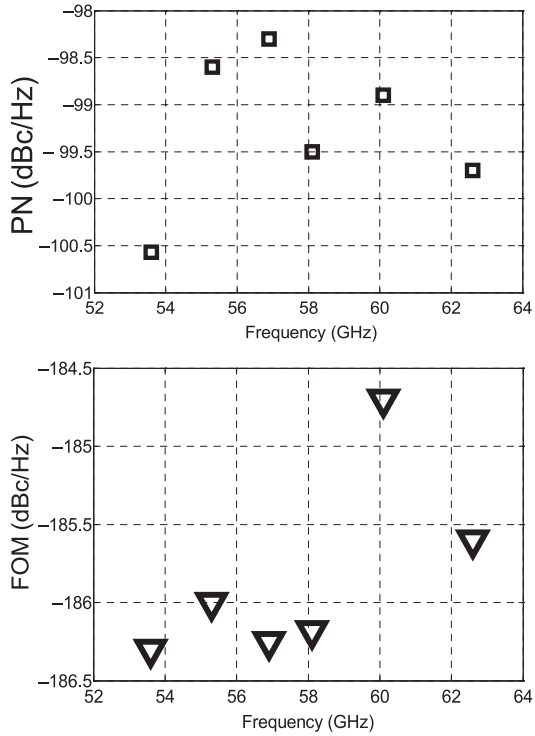

Fig. 19. Measured phase noise (at 1 MHz offset) and FoM versus SMV output frequency.

Table III presents the simulation results for an *iso-swing* design comparison, from which several conclusions can be drawn.

1) Although F-VCO has reduced power consumption and design complexity by needing only one stage of buffer amplification, the performance is poor in terms of PN and FTR.
2) Although the 2H-VCO (or F-VCO) does not need to generate any second harmonic which suffers from smaller voltage swing, the lower Q_{tank} at 30 GHz (or 60 GHz) compared to 20 GHz degrades the PN significantly.
3) The VCO core experiences a higher capacitive loading in the 2H-VCO topology compared to the 3H-VCO, lowering the FTR.
4) The VCO cores operating at higher frequencies must be operated with a larger current from the supply to ensure oscillation startup.

We observe that even when accounting for signal swing, the 3H-VCO with an active mixer has the best performance in terms of PN, tuning range and total power consumption.

IV. Measurement Results

The 3H-SMV shown in Fig. 10(b) is designed and fabricated in a 0.13 μm CMOS process. The core Class-C VCO is designed to operate between 17 and 21 GHz; the mixer and the output buffer at 60 GHz. For this prototype, a large signal swing into a capacitive load is not a design constraint. Instead, a single stage output buffer is designed to drive the 50 Ω load of the test equipment so that a comparison can be made to the state-of-the-art designs. The VCO varactor is implemented using a thick oxide accumulation MOS varactor. Both L_{Bias}

TABLE IV
MEASURED PERFORMANCE SUMMARY OF STATE-OF-THE-ART MILLIMETER-WAVE VCOS

Parameters	Architecture	Freq. (GHz)	FTR %	PN (dBc/Hz) @ 1 MHz PN (dBc/Hz) @ 10 MHz	V_{DD} (V)	P_{DC} (mW)	Buffered P_{OUT} (dBm)	Tech. (nm) CMOS process	FoM (dBc/Hz) FoM_T (dBc/Hz)
This Work H-VCO	Class-C self-mixing VCO (SMV)	52.8–62.5	16.8	–100.57@53.6 GHz –124.75@53.6 GHz	1.2	7.6 4.1 VCO + 3.5 Mixer	–28@52.8 GHz, –31@62 GHz	130	–186.3 –190.85
[1] 3H-VCO	Transformer-based 3rd order extractor	58	25.4	–100.1 –122.3	1	13.5	NA	40	181.5 189.6
[2] F-VCO	Class-B Inductive peaking	64	8.7	–95 NA	0.6	3.16	–20@64 GHz	90	–186 –185
[3] 3H-VCO	Triple-push VCO	67.8	13.6	NA –95	1.4	18	–36.4@63.2 GHz	130	–159 –161.7
[8] F-VCO	Dual mode tank	66.1	27.9	NA –103	1	13	–31@75 GHz	65	–168 –177
[12] 3H- ILO	Injection-locked	60.5	8.2	–95* –113*	1.2	>33.6 (VCO+ILO)	–10@60.48 GHz*	65	–175 –173.4
[27] F-VCO	Class-B DCO	57	11.6	–92 NA	1.2	13.2	NA	65	176.4 177.7
[26] F-VCO	Inductive divider feedback	54	9.1	–95 –119.2	1	24	NA	65	–179.8 –179
[28] F-VCO	Magnetically tuned multimode	73.8	41	NA –104.6 to–112.2	1.2	8.4 – 10.8	NA	65	–172 to–180 –184 to–192.2
[29] F-VCO	Inductive-division LC tank	61.7	4.81	–90 NA	0.43	1.2	NA	90	–185 –178.6
[30] F-VCO	CMOS VCO	70.2	9.55	NA –106.14	1	5.4	—37@73 GHz	65	–175.76 –175.36
[31] F-VCO	Transformer-based dual-band	67.9	19.8	NA –105.8 to–112	1.2	1.44	NA	65	–173.8 to –180.4 –180 to –187.4
[32] F-VCO	Magnetically coupled	59.3	39	NA –101.7 to–113.4	1	8.9 – 10.4	–31@75 GHz	65	–167.8 to –179 –179.6 to 190.6

*includes off-chip amplification

and L_B are implemented using a $\lambda/4$ transmission-line. All transmission-lines and inductors are modeled and simulated using *Momentum* planar electromagnetic software.

Fig. 15 shows the die micrograph. The active die area (excluding pads) is about 300×670 μm^2. The device under test (DUT) is directly probed as shown in Fig. 15 (using 50–67 GHz *Cascade infinity* probes) and measured with R&S signal and spectrum analyzer. To minimize noise contribution of the supply, a battery-based source is used for the supply and control voltage of the varactors [24]. The output signal power of SMV is -31 dBm measured at the maximum output frequency of 62.48 GHz, as shown in Fig. 16. Fig. 17 shows the tuning range plot of the SMV, spanning from 52.8 to 62.5 GHz with an FTR of 16.8%.

Fig. 18 shows the measured PN plot of SMV at mid-band carrier frequency of 53.68 GHz with a PN of -100.6 dBc/Hz at 1 MHz and -124.8 dBc/Hz at 10 MHz offset, respectively. The variation in the PN, measured at 1 MHz offset frequency from the carrier, is shown in Fig. 19(a) across the entire tuning range of the VCO. The overall variation is about 2 dB. Fig. 19(b) shows the corresponding variation in the FoM across the tuning range.

The performance summary of the Class-C SMV architecture and its comparison to the state-of-the-art designs is presented in Table IV.

V. CONCLUSION

An SMV architecture is described for mm-wave applications. The structure uses a push–push Class-C VCO for low PN, high tuning range, and higher first- and second-harmonic content, and then mixes these two harmonics to generate the third harmonic as the desired output. We refer to this architecture as 3H-VCO. Analyses and simulations confirm that this indirect LO signal generation technique has superior tuning range and PN performance as compared to those of direct synthesis techniques. As a proof-of-concept, a 60 GHz 3H-VCO prototype is designed and fabricated in a 0.13 μm CMOS process. The measured performance of the implemented 60 GHz prototype compares favorably with the state-of-the-art designs.

APPENDIX

Consider the drain current of a short-channel device operating in saturation region [25]

$$I_D = \frac{1}{2}\mu_n C_{\rm ox} W E_{\rm sat}(V_{\rm GS} - V_{\rm th}) = K_n W (V_{\rm GS} - V_{\rm th}) \quad \text{(A1)}$$

where μ_n is carrier mobility, $C_{\rm ox}$ is the gate oxide capacitance per unit area, W is the channel width, $E_{\rm sat}$ is the electric field at which the carrier velocity drops to half the value extrapolated from weak-field mobility, and $V_{\rm th}$ is the threshold voltage. $I_D(t)$ for a transistor working in a Class-C core can be written as

$$I_D(t) = \begin{cases} \frac{1}{2}\mu_n C_{\rm ox} W E_{\rm sat} \\ \quad (V_{\rm GS,dc} + A\cos(\omega_0 t) - V_{\rm th}) & -\varphi + 2k\pi \le \omega_0 t \le \varphi + 2k\pi \\ 0 & \text{elsewhere} \end{cases} \quad \text{(A2)}$$

where A is the oscillation amplitude and $\Phi_C = 2\varphi$ is the conduction angle, given by

$$\Phi_C = 2\cos^{-1}\left(\frac{V_{\mathrm{GS,DC}} - V_{\mathrm{th}}}{A}\right). \tag{A3}$$

Using the Fourier expansion of $I_D(t)$, the dc term can be calculated as

$$\begin{aligned} I_{\mathrm{dc}} &= \frac{1}{2\pi}\int_{-\varphi}^{\varphi}\frac{1}{2}\mu_n C_{\mathrm{ox}} W E_{\mathrm{sat}} A(\cos(\alpha)-\cos(\varphi))d\alpha \\ &= \frac{1}{2\pi}\mu_n C_{\mathrm{ox}} W E_{\mathrm{sat}} A[\sin(\varphi)-\varphi\cos(\varphi)]. \end{aligned} \tag{A4}$$

Similarly, the magnitude of the $\mathrm{n}f_0$ harmonic component is given by

$$\begin{aligned} I_n &= \frac{1}{\pi}\int_{-\varphi}^{\varphi}\frac{1}{2}\mu_n C_{\mathrm{ox}} W E_{\mathrm{sat}} A(\cos(\alpha)-\cos(\varphi))\cos(n\alpha)d\alpha \\ &= \frac{1}{2\pi}\mu_n C_{\mathrm{ox}} W E_{\mathrm{sat}} A\left(\frac{\sin(n+1)\varphi}{n+1}+\frac{\sin(n-1)\varphi}{n-1}\right. \\ &\quad \left.-\frac{2}{n}\cos(\varphi)\sin(n\varphi)\right). \end{aligned} \tag{A5}$$

Thus, the dc-to-nf_0 current efficiency, $\eta_{I,n}$ is calculated as

$$\eta_{I,n} = \left|\frac{\mathrm{sinc}\left(\frac{(n-1)\varphi}{\pi}\right)+\mathrm{sinc}\left(\frac{(n+1)\varphi}{\pi}\right)-2\cos\varphi\,\mathrm{sinc}\left(\frac{n\varphi}{\pi}\right)}{\mathrm{sinc}\left(\frac{\varphi}{\pi}\right)-\cos(\varphi)}\right| \tag{A6}$$

where the normalized sinc function is defined as $\mathrm{sinc}(x) = \sin(\pi x)/\pi x$.

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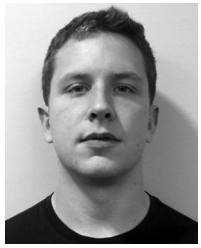

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