Impact of Custom Interconnect Masks on Cost and Performance of Structured ASICs

Final Doctoral Exam

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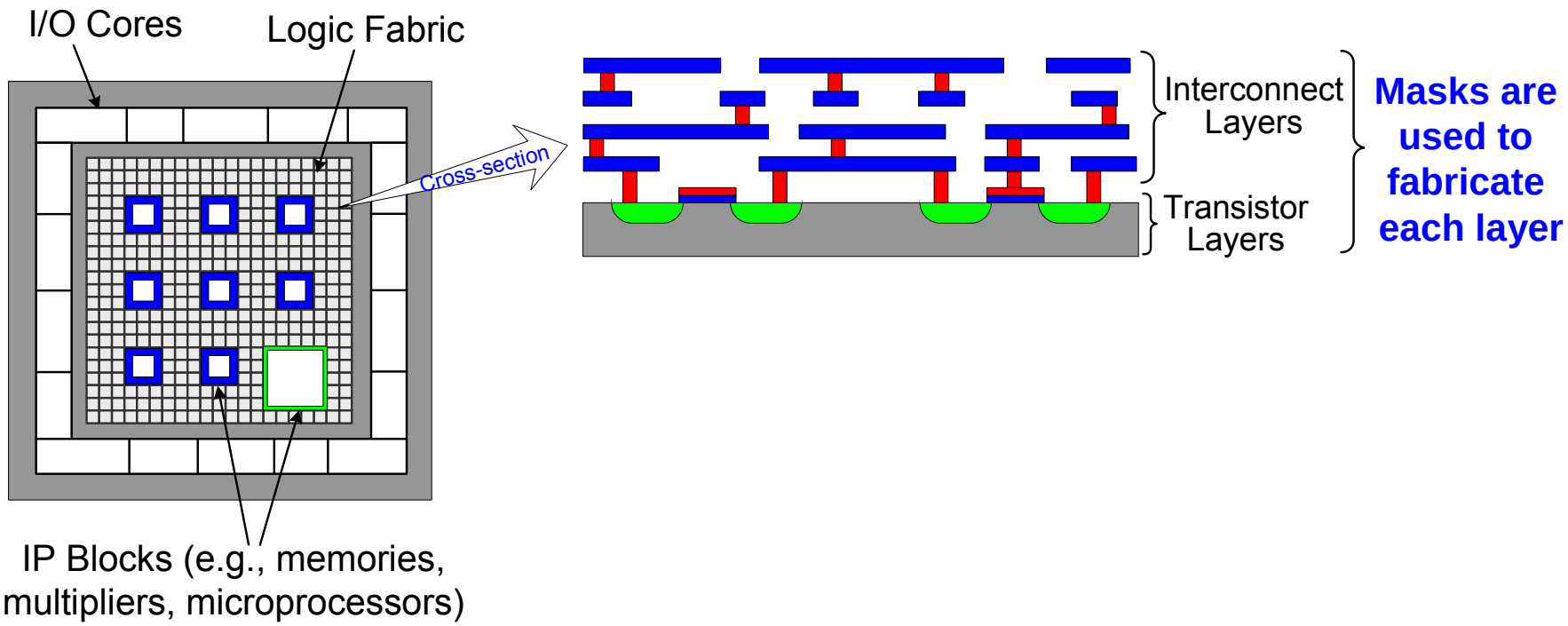
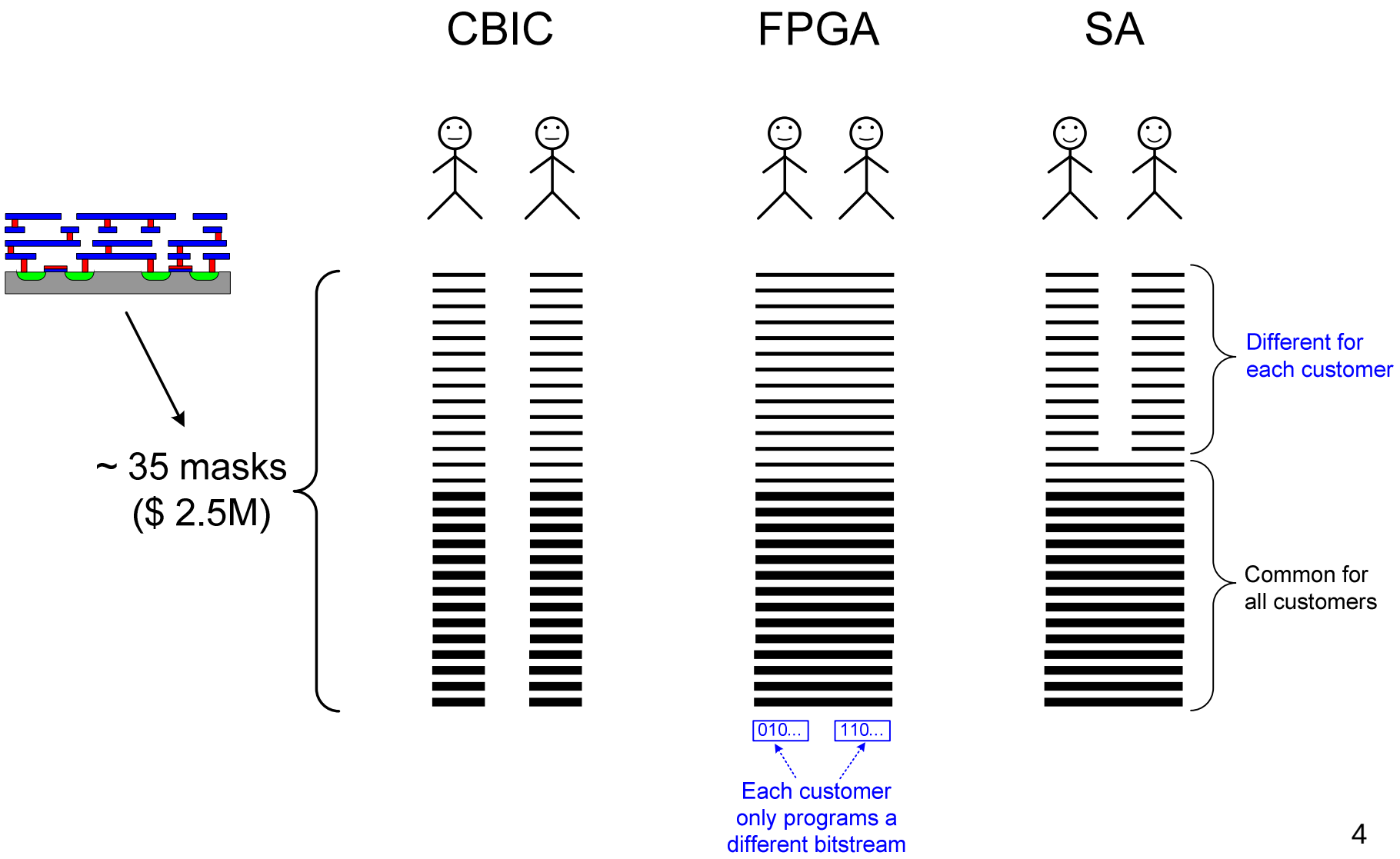
Overview

- Motivation
- Research Problem
- Previous Work
- Contributions
  - Cost Model to Estimate Structured ASIC Die-cost
  - Structured ASIC Evaluation Framework
  - Area, delay, power, and die-cost trends for Structured ASICs
- Limitations and Future work

Motivation


I/O Cores
Logic Fabric
Cross-section
IP Blocks (e.g., memories, multipliers, microprocessors)
Interconnect Layers
Transistor Layers
Masks are used to fabricate each layer

Motivation


CBIC
FPGA
SA
~ 35 masks
($ 2.5M)
Different for
each customer
Common for
all customers
010...
110...
Each customer
only programs a
different bitstream

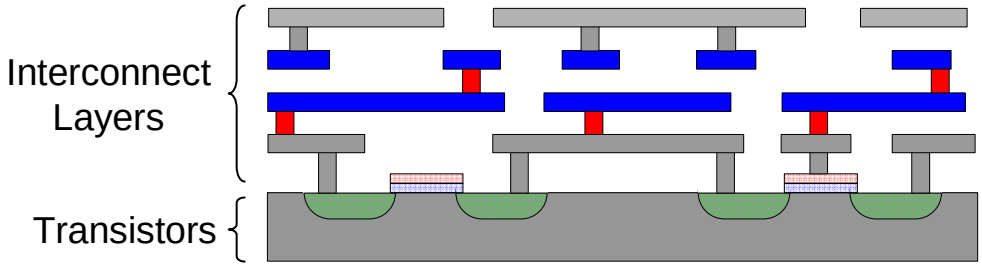
Research Problem

How is the *cost* and *performance* of Structured ASICs affected by the number of *custom masks*?

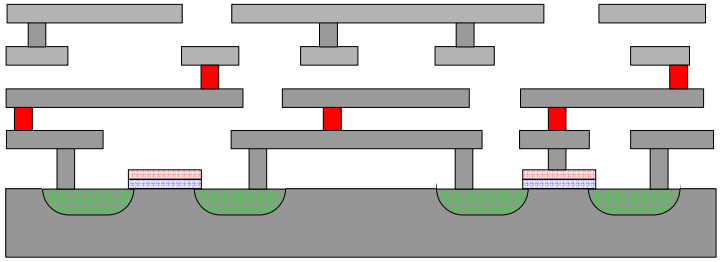
Types of Structured ASICs

- Which masks need to be customized?

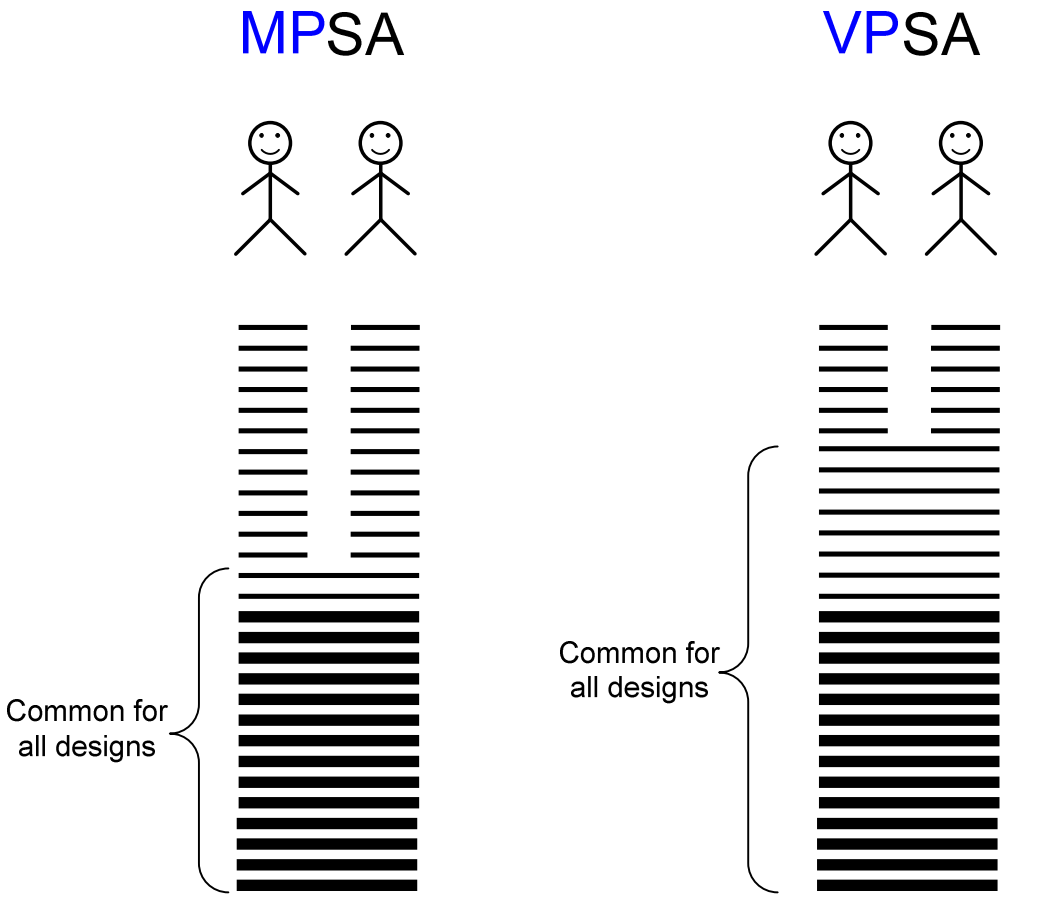
Metal-and-via Programmable
(MPSA)



Via Programmable
(VPSA)



Types of Structured ASICs



- Custom Metal Masks
  - → Lower Power
  - → Faster
  - → Smaller Area
- MPSA vs VPSA Cost ??

Previous Work

- Academic Efforts
  - Ran & Sadowska: VPSA logic and interconnect fabrics
  - Pillegi et al. and Koorapaty et al.: VPSA logic block
  - Kheterpal et al.: VPSA interconnect fabrics
  - Veredas et al.: MPSA (Zelix)
  - Nakamura et al.: VPSA (VPEX)
  - Chau et al.: VPSA logic block
- Point solutions
  - Logic block and routing fabrics with fixed configurability

Previous Work

- Commercial Efforts
  - Point Solutions
  - Mostly MPSAs
  - Wide range for configurability
  - Products with high configurability have been discontinued

State	Company	Product	Type	Custom Layers (M: metal, V: via)
Active	Altera	Hardcopy Series	MPSA	2M
	eASIC	Nextreme Series	VPSA	1V
Semi-Active	ChipX	CX6200	MPSA	2–4M
	Faraday	MPCA	MPSA	3M + 2V
	ON Semi-conductor	Xpress Array-II	MPSA	?
	ViASIC	ViaMask, DuoMask	VPSA	1–2V
	Virage Logic	ASAP	MPSA	3–4M
Defunct	Fujitsu	AccelArray	MPSA	3–4M
	Lightspeed	-	MPSA	2M+2V to 6M+6V
	LSI Logic	RapidChip	MPSA	all-M + all-V
	NEC	ISSP	MPSA	2M
	Tier Logic	-	-	?

Contributions

1. Cost Model to Estimate Die-cost of Structured ASICs
2. Structured ASIC Evaluation Framework
3. Area, Delay, Power, and Die-cost Trends for Structured ASICs

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Structured ASIC Die-Cost

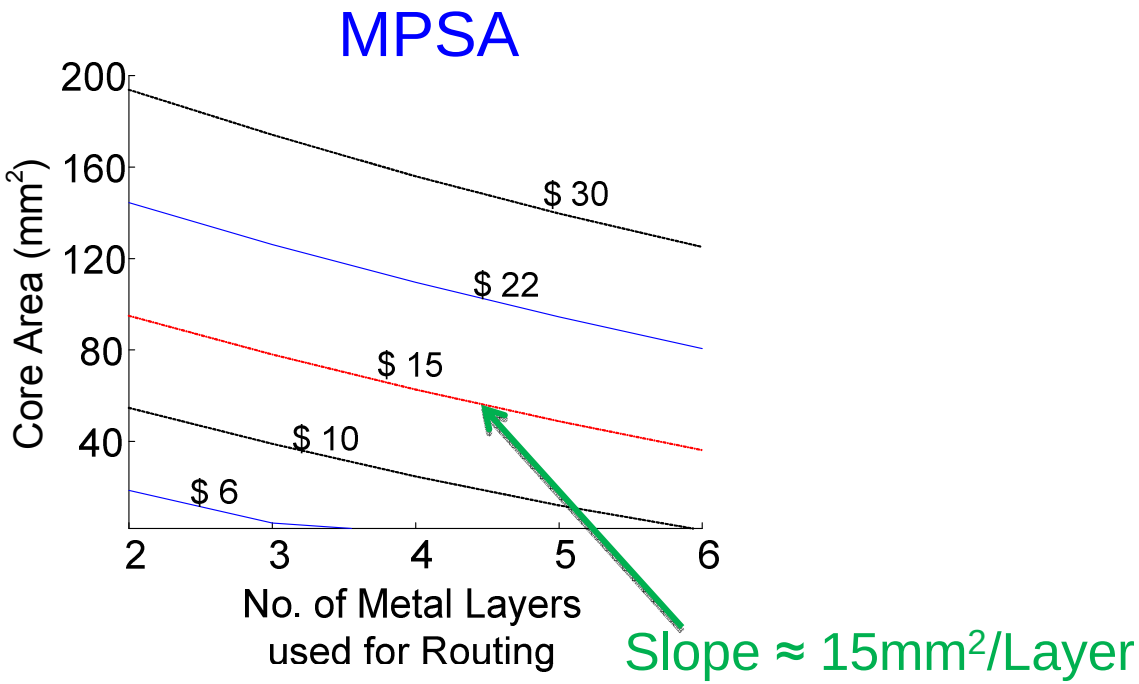
- Primary cost components
  - Die Area
  - Number of configurable layers *(New for structured ASICs)*
    - *Metal layers used for routing*
    - *Configured by one or more via, or metal-and-via masks*
- Secondary cost components
  - Die Yield
  - Mask-set and processing costs
  - Volume requirements

Cost Model

$$Cost_{die} = Area \times K_0 + Config.\ Layers \left(Area \times K_1 + K_2 \right) + K_3$$

- Variables
  - Die Area and Yield
  - Configurable layers
- Constants
  - Mask/wafer processing cost
  - Volume requirements
  - Architecture Related

Cost Model



- At constant cost, area can be traded for number of customizable layers

Contributions

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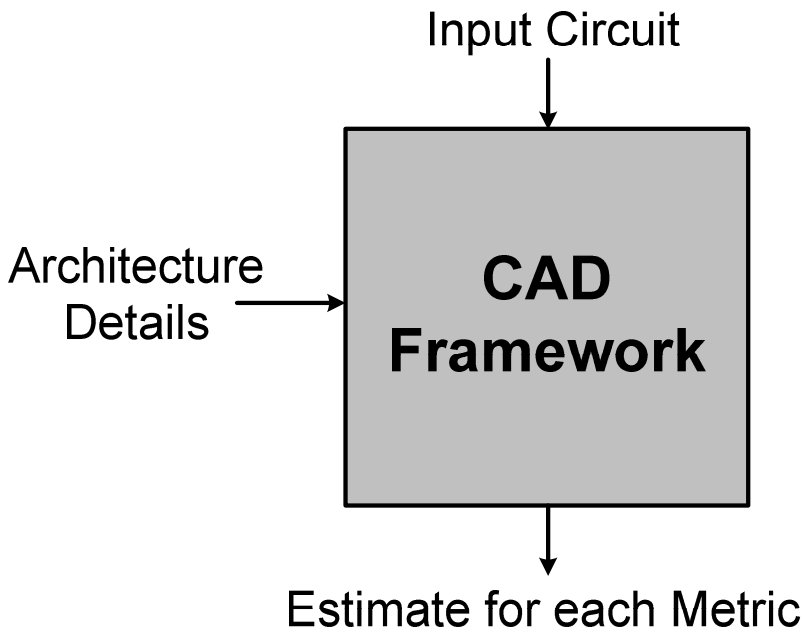
Structured ASIC Evaluation Framework

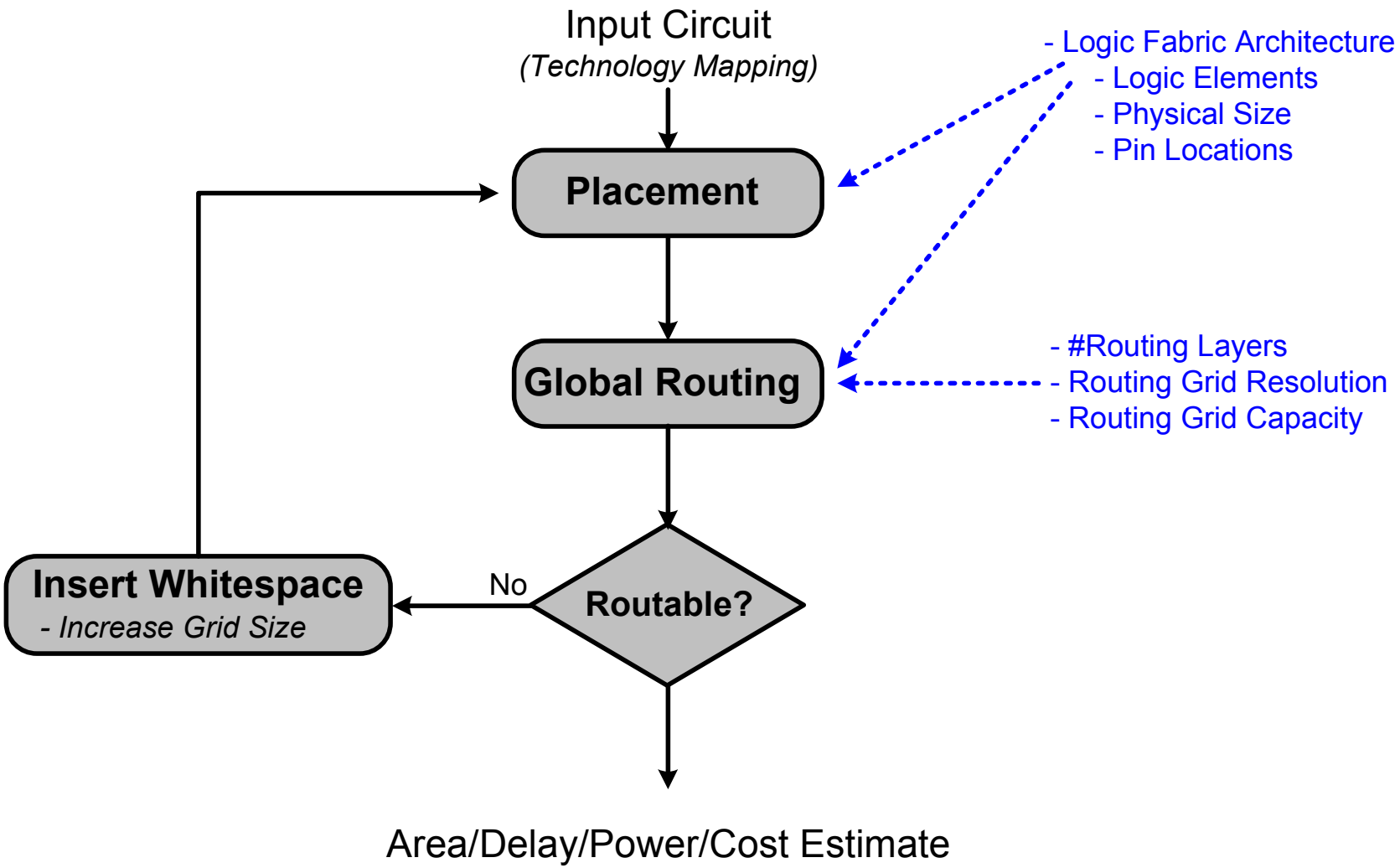
- Architecture Modeling
  - Logic Fabric
  - Interconnect Fabric
- Metrics
- CAD Flow



Metrics

- Cost
  - Detailed cost model (just presented)
- Area
  - Chip Area
- Delay
  - Average net delay (Elmore model)
- Power
  - Total metal + via capacitance

CAD Overview



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Performance and Cost Trends

- MPSAs
  - Two Benchmark Suites
    - Homogeneous (MCNC) Circuits
    - Heterogeneous (eASIC) Circuits
  - Comparison to CBIC costs
  - Impact of Whitespace Insertion
- VPSAs
  - Fixed-metal Routing Fabrics
  - Impact of Logic Block Pin Positions
  - Power, Delay, Area, and Die-cost
  - Comparison to MPSAs

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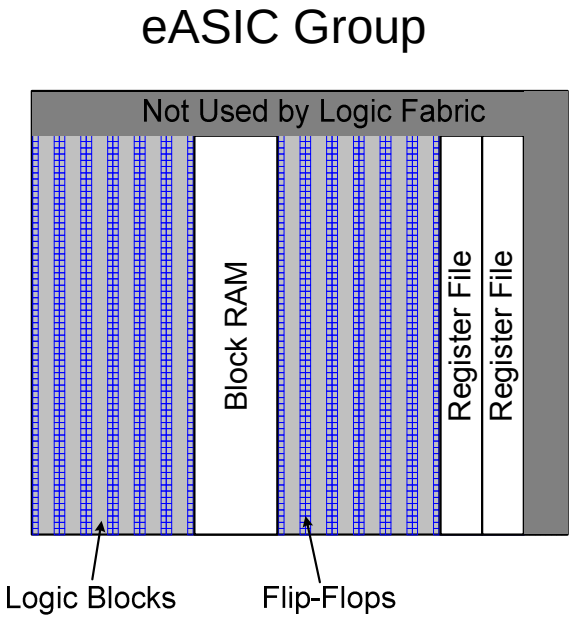
Trends for Heterogeneous Circuits

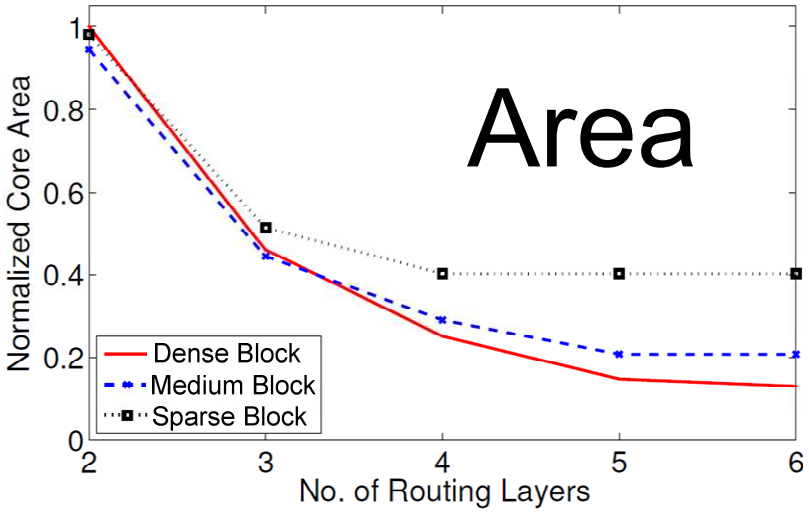
- Device Architecture
  - Logic Elements
    - eCell, eDff, BlockRAM, RegFile
- Circuits
  - Up to 1 Million logic blocks
- Placement Enhancement
  - Different logic elements
- Layout Effort
    - Dense
    - Medium
    - Sparse



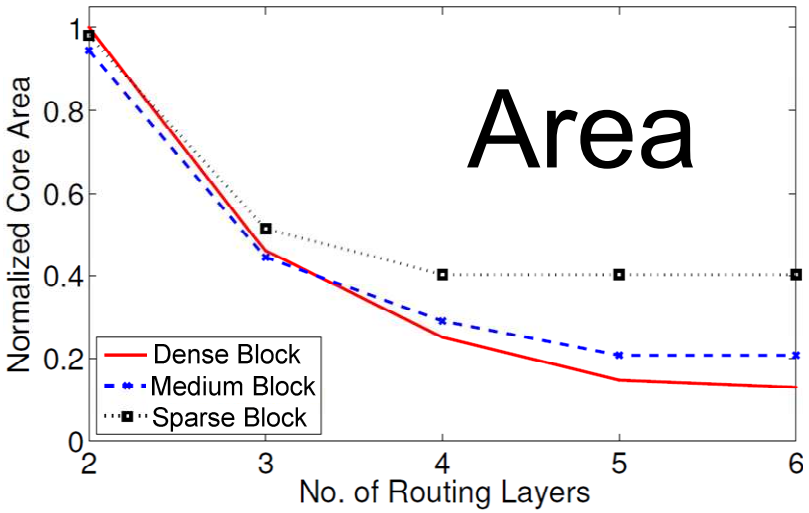
Trends for Heterogeneous Circuits

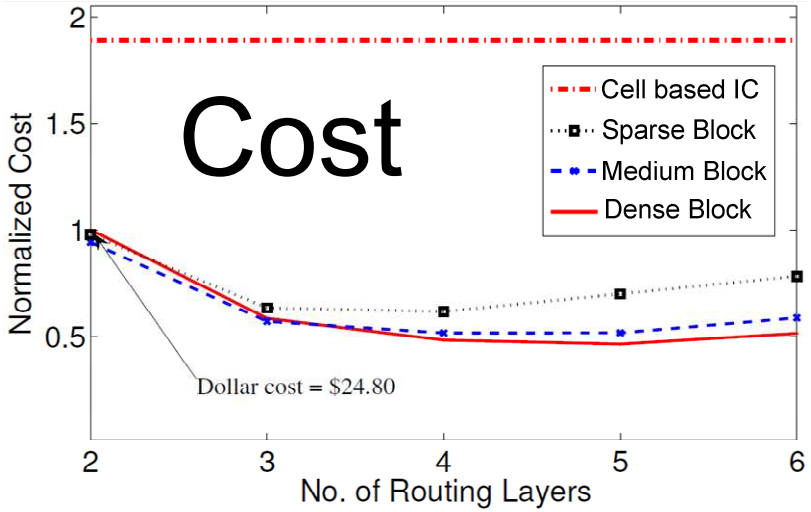
- Area and Die-Cost

Trends for Heterogeneous Circuits



Trends for Heterogeneous Circuits





– Lowest cost obtained with 3 or 4 layers
– More than 4 layers offer little advantage

Performance and Cost Trends

- MPSAs
  - Two Benchmark Suites
    - Homogeneous (MCNC) Circuits
    - Heterogeneous (eASIC) Circuits
  - Comparison to CBIC costs
  - Impact of Whitespace Insertion
- VPSAs
  - Fixed-metal Routing Fabrics
  - Impact of Logic Block Pin Positions
  - Power, Delay, Area, and Die-cost
  - Comparison to MPSAs

Trends for VPSAs

- Routing Fabrics *(by Ran & Sadowska)*
  - Crossover
  - Jumper20, Jumper40
  - SingleVia

  n-1 custom via layers

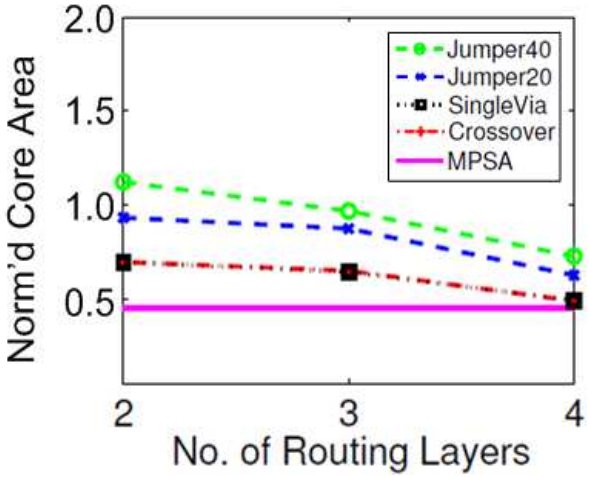
  1 custom via layer

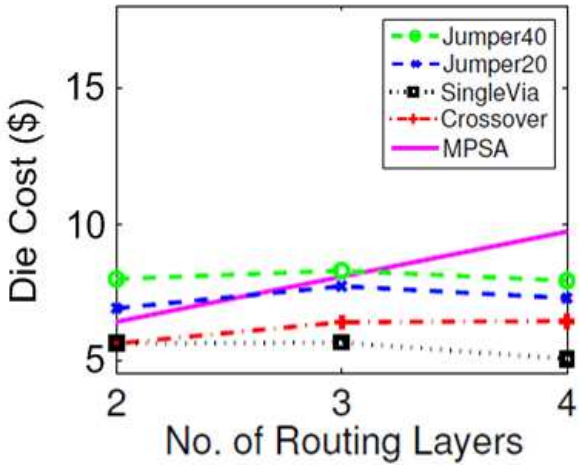
  n fixed-metal layers
- Logic Blocks
  - Logic Capacity
    - *2-in,1-out* to *16-in,8-out*
  - Layout Effort
    - Dense
    - Medium
    - Sparse

VPSA Area and Die-cost Example

- Logic Block
  - Logic Capacity: 2-in, 1-out
  - Layout Effort: Medium
- MPSAs: Small Area

  VPSAs: Lower Cost
- Gap between different VPSA Fabrics





VPSA Area and Die-cost Trends

- Key Observations

		Delay Trends	Power Trends	Area Trends	Cost Trends
VPSAs	Crossover Fabric	–	–	–	–
	Jumper Fabric	0 to 89% worse than Crossover	0 to 85% worse than Crossover	0 to 60% worse than Crossover	–
	SingleVia Fabric				0 to 36% cheaper than VPSAs with other fabrics
MPSAs vs. VPSAs		MPSAs 1 to 10x better than VPSAs	MPSAs 1 to 3.5x better than VPSAs	MPSAs 1 to 5x better than VPSAs	MPSAs are cheaper only for Dense Logic Blocks with 2 or 3 layers. VPSAs are up to 50% cheaper in other cases

Contributions

1. Cost Model to Estimate Die-cost of Structured ASICs
2. Structured ASIC Evaluation Framework
3. Area, Delay, Power, and Die-cost Trends for Structured ASICs

Limitations

- Uniform Whitespace Distribution
- No Buffer Insertion
- No Detailed Logic Block Architectures
  - “Approximate” Technology Mapping
  - Delay and Power of Logic Blocks
  - Critical Path Delay
- Logic Block Configuration Schemes
- Overhead of Power and Clock Networks

Future Work

- Short term
  - Congestion-driven Whitespace Insertion
  - Impact of Buffer Insertion
  - Efficient Algorithm for VPSA Detailed Routing
  - Timing and/or Power Aware CAD Flows
  - New Logic and Interconnect Fabrics
- Long term
  - Improved Manufacturability
  - Ease of Design

Publications

- Refereed Journal Publication

  U. Ahmed, G. Lemieux, S. Wilton, " **Performance and Cost Tradeoffs in Metal-Programmable Structured ASICs (MPSAs),"** IEEE Transactions on VLSI Systems, 2010.
  Available Online: http://dx.doi.org/10.1109/TVLSI.2010.2076841

- Refereed Conference Publications

  U. Ahmed, G. Lemieux, S. Wilton, "**Area, Delay, Power and Cost Trends for Metal-Programmable Structured ASICs (MPSAs)**," International Conference on Field-Programmable Technology (ICFPT'09), Dec. 2009.

  U. Ahmed, G. Lemieux, S. Wilton, "**The Impact of Interconnect Architecture on Via-Programmed Structured ASICs (VPSAs)**," International Symposium on Field-Programmable Gate Arrays (FPGA 2010), Feb. 2010.

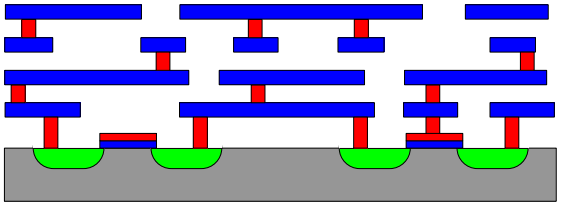
- In Preparation

  U. Ahmed, G. Lemieux, S. Wilton, "**Performance and Cost Tradeoffs in Via-Programmable Structured ASICs (VPSAs),"** to be submitted to IEEE Transactions on VLSI Systems.

Structured ASIC Vendor and User

Vendor designs and fabricates a portion of the device

- User runs CAD tools to generate the required data for the masks
- Cannot make architectural decisions



Vendor prepares the necessary masks and fabricates the remaining portion of the device

Cost Comparison

	FPGA	Structured ASIC	CBIC
Total Design Cost	$\sim \$165k$	$\sim \$500k$	$\sim \$5.5M$
Vender NRE	None	$\sim \$100k - \$200k$	$\sim \$1M - \$3M$
#Tools Required	2 to 3	2 to 3	6 to 10
Cost of Tools	$\sim \$30k$	$\sim \$120k - \$250k$	$> \$300k$
#Engineers	1 to 2	2 to 3	5 to 7
Price per chip	$\$220 - \$1k$	~$30 to $150	$\sim \$ 30$
Total Unit Cost (Qty: 1k)	$\sim \$1000$('03)	$\sim \$500 - \$650$	$\$55k$
Total Unit Cost (Qty: 5k)	$\sim \$220$(4Q'04)	$\sim \$100 - \$150$	$\$1.1k$
Total Unit Cost (Qty: 500k)	$\sim \$40$(4Q'04)	$> \$21$	$\$11 - \$20$

Cost Model

$$Cost_{die} = C_{base} +$$

$$C_{custom} +$$

$$C_{proto}$$

Cost Model

$$Cost_{die} = \textit{Cost of the masks for the base (common portion)} + \textit{Cost of fabricating the base portion} +$$

$$C_{custom} +$$

$$C_{proto}$$

Cost Model

$$Cost_{die} = \textit{Cost of the masks for the base (common portion)} + \textit{Cost of fabricating the base portion} +$$

$$\textit{Cost of the remaining masks} + \textit{Cost of fabricating the remaining portion} +$$

$$C_{proto}$$

Cost Model

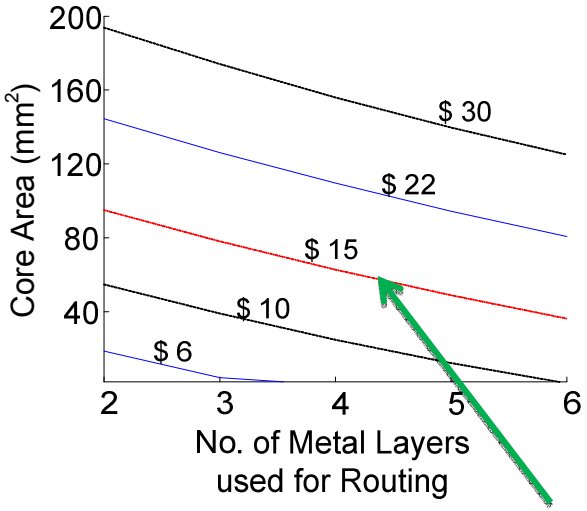
$Cost_{die}$ = *Cost of the masks for the base (common portion)* + *Cost of fabricating the base portion* +

Cost of the remaining masks + *Cost of fabricating the remaining portion* +

Similar to C_{custom}*, but depends on the number of spins*

Cost Model

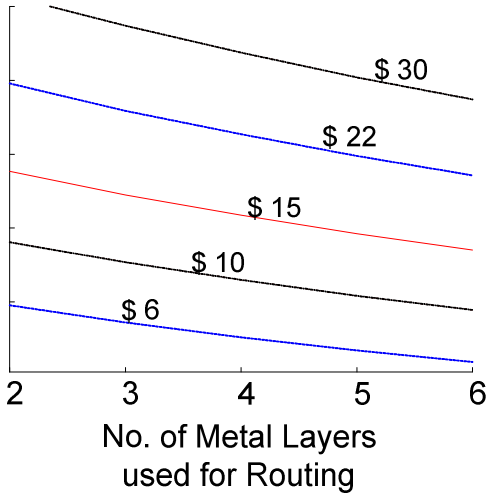
MPSA



Slope ≈ 15mm²/Layer

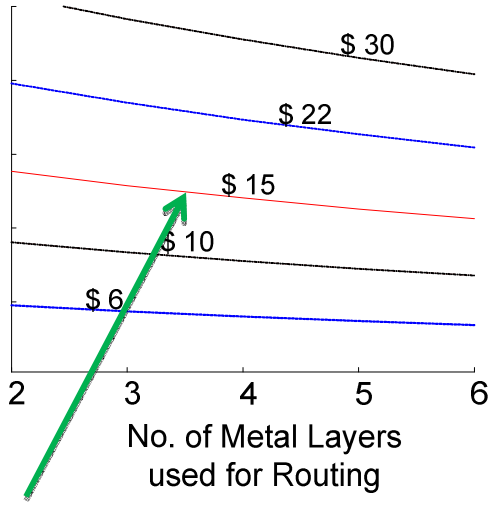
VPSA

(Multiple Via Layers)



VPSA

(Single Via Layer)

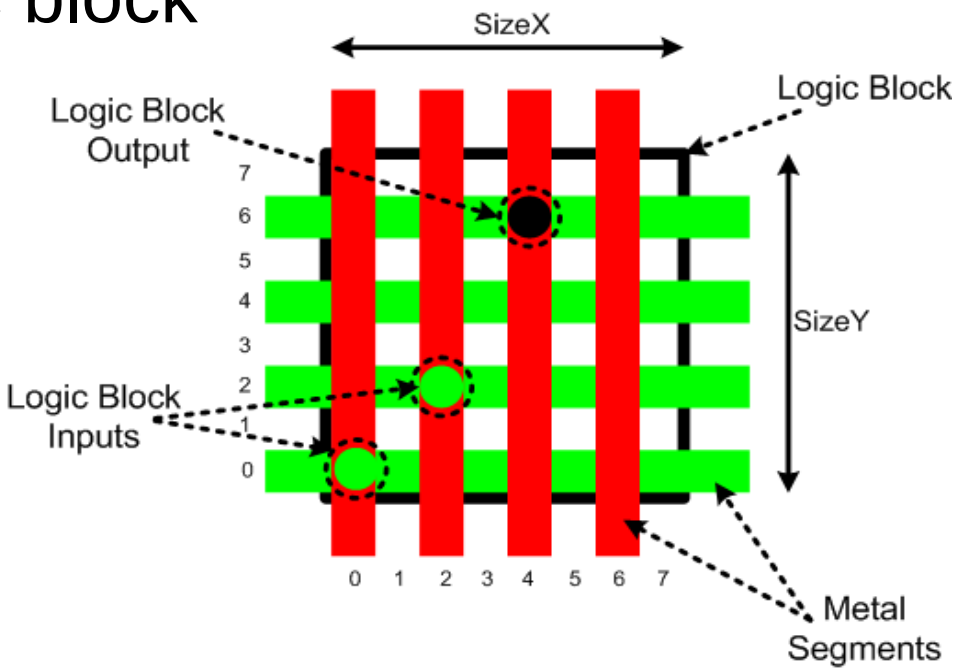


Slope ≈ 6mm²/Layer

- At constant cost, area can be traded for number of customizable layers

Logic Block Model

- Characteristics of logic block
  - Physical dimensions (in wire pitches)
  - Pin locations
- Do not need low-level layout details



Parameterize Logic Block

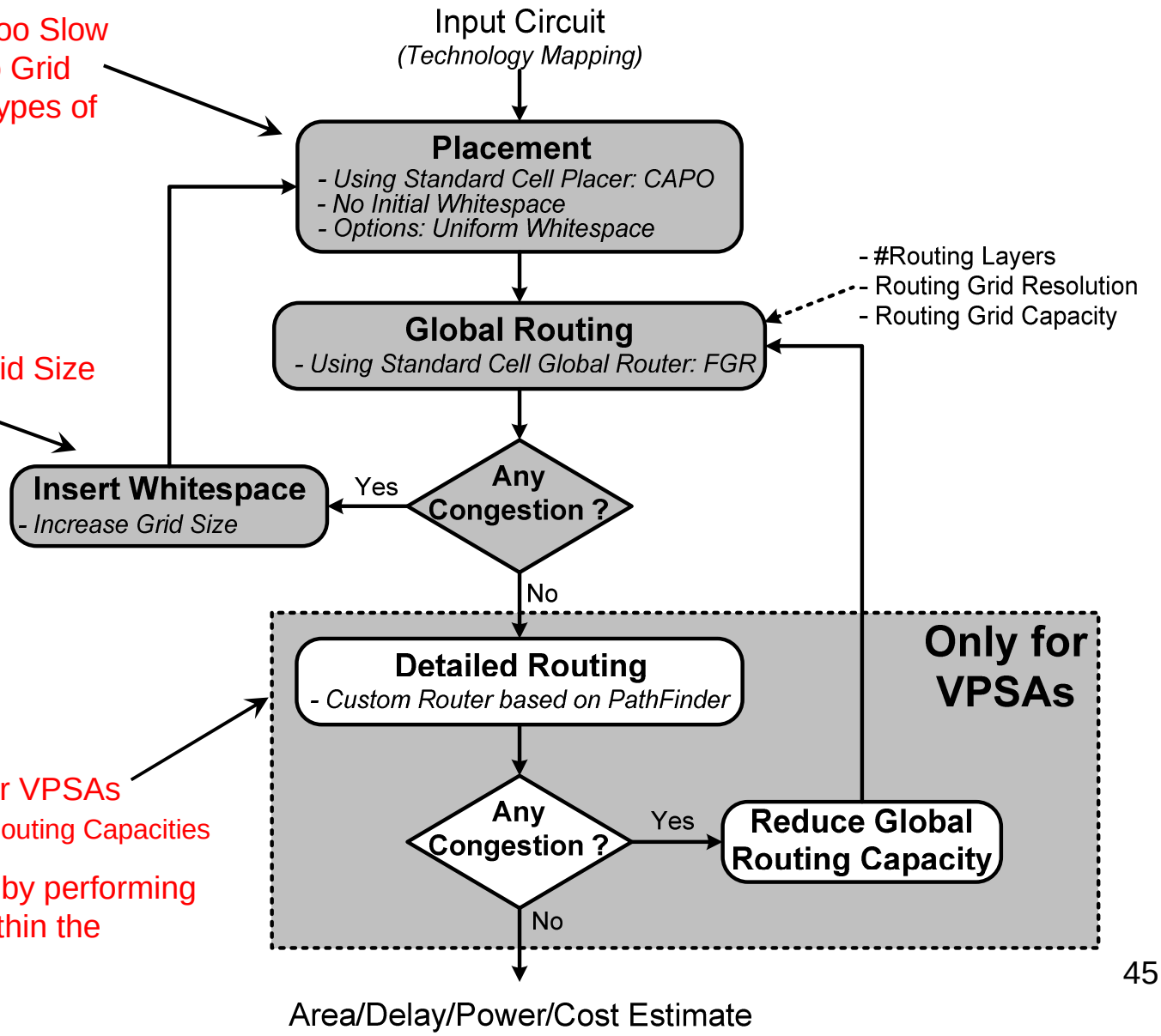
- Cover wide search space for logic blocks
- Vary layout density
  - **Dense**: Determined by # pins (small layout area)
  - **Sparse**: Determined by Standard Cell implementation
- Vary logic capacity
  - Sweep number of inputs and outputs
    - 2-input, 1-output logic blocks (shown here)
    - 16-input, 8-output logic blocks (also in paper)
  - Use logic clustering (T-VPack) as tech-mapper

Interconnect Model

- MPSAs
  - Set of equally-wide and equally-spaced horizontal or vertical wires for each configurable layer
- VPSAs
  - Detailed architecture specified for a basic tile
    - Metal segments (start, end positions)
    - Potential via sites (fixed or configurable vias)

CAD Framework for Structured ASICs

- Simulated Annealing Too Slow
- Logic Cells Snapped to Grid
- Can Handle different Types of Logic Blocks

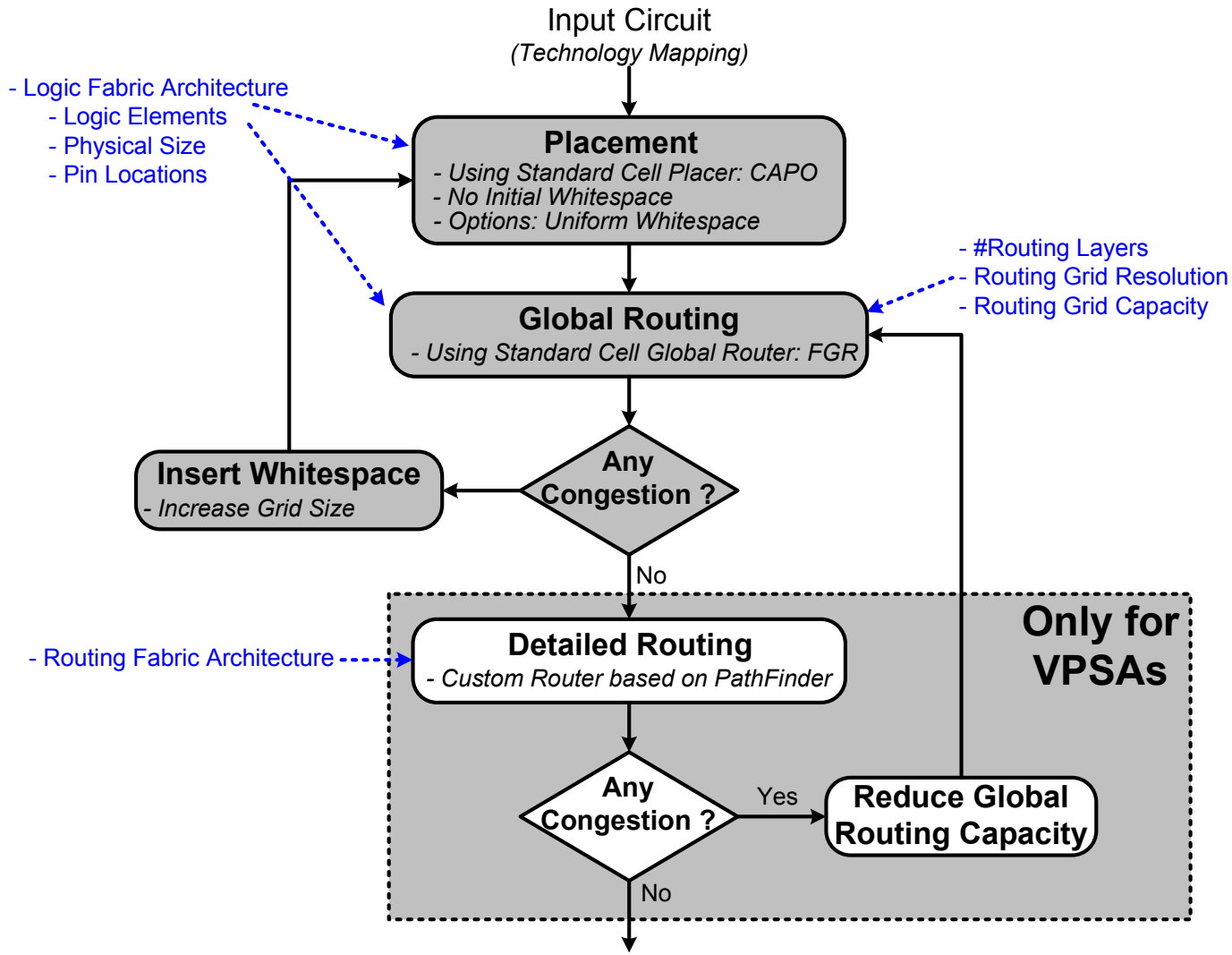


- Increase Placement Grid Size

- Detailed routing only for VPSAs
  - Difficult to find Global Routing Capacities

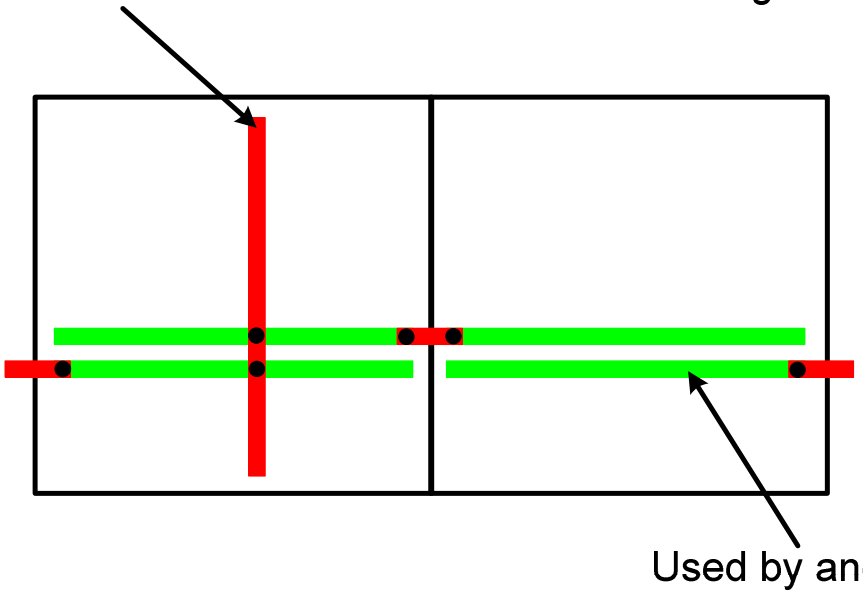
- Limit the search space by performing detailed routing only within the Global Route

CAD Framework



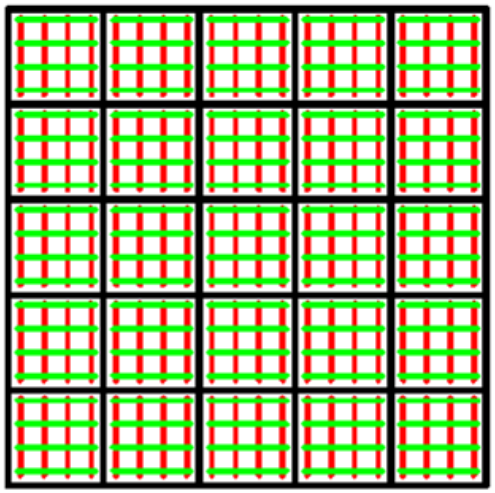
MPSA vs. VPSA Detailed Routing

The entire segment is used only in switching from one track position to another in the underlying layer. This reduces the number of tracks available for routing



Impact of Whitespace Insertion

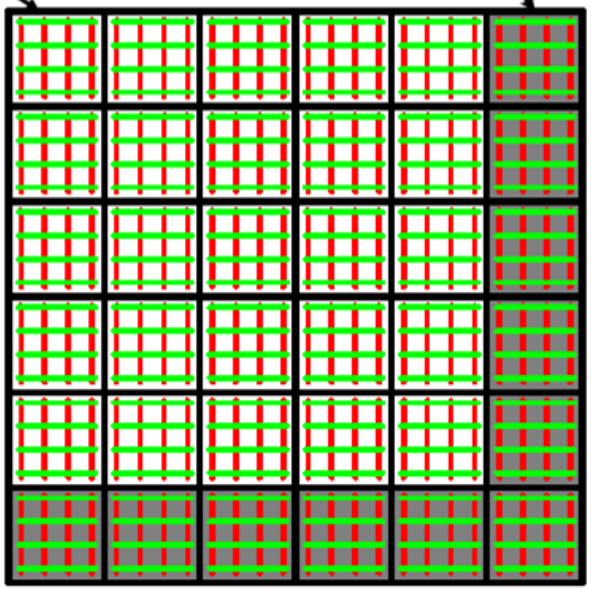
- Estimated using Routing Capacity



- Placement Grid: 5x5
- Routing Layers: 4
- Routing Tracks Over Logic Block: 4
Total Routing Capacity = 5x5x4x4
= 400

Original Grid
Capacity with 3 layers = 5x5x4x3
= 300

Blocks Added to Increase Routing Capacity

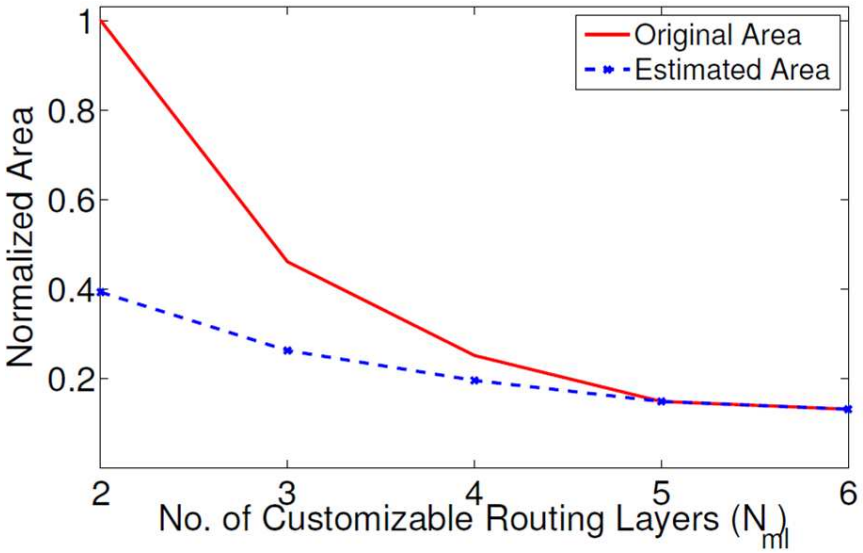


- Placement Grid: 6x6
- Routing Layers: 3
- Routing Tracks Over Logic Block: 4
Total Routing Capacity = 6x6x4x3
= 432

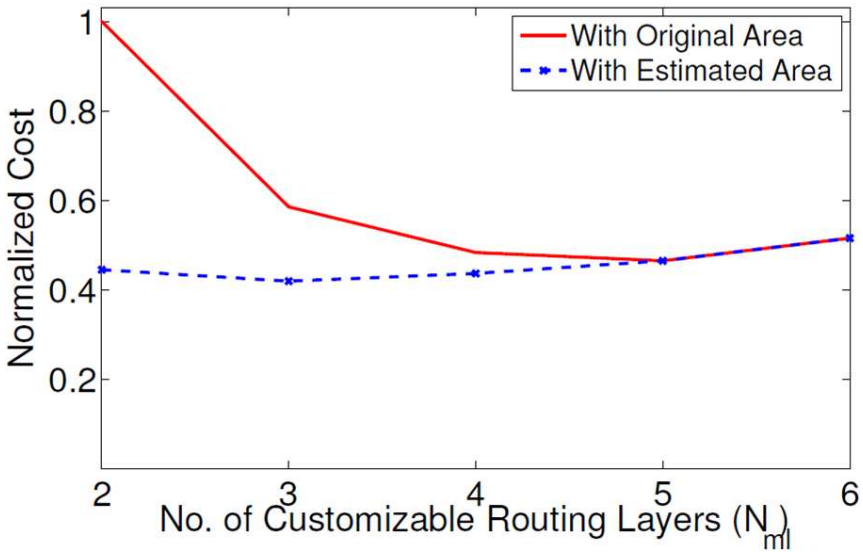
Impact of Whitespace Insertion

- Area and Die-cost

Small Block



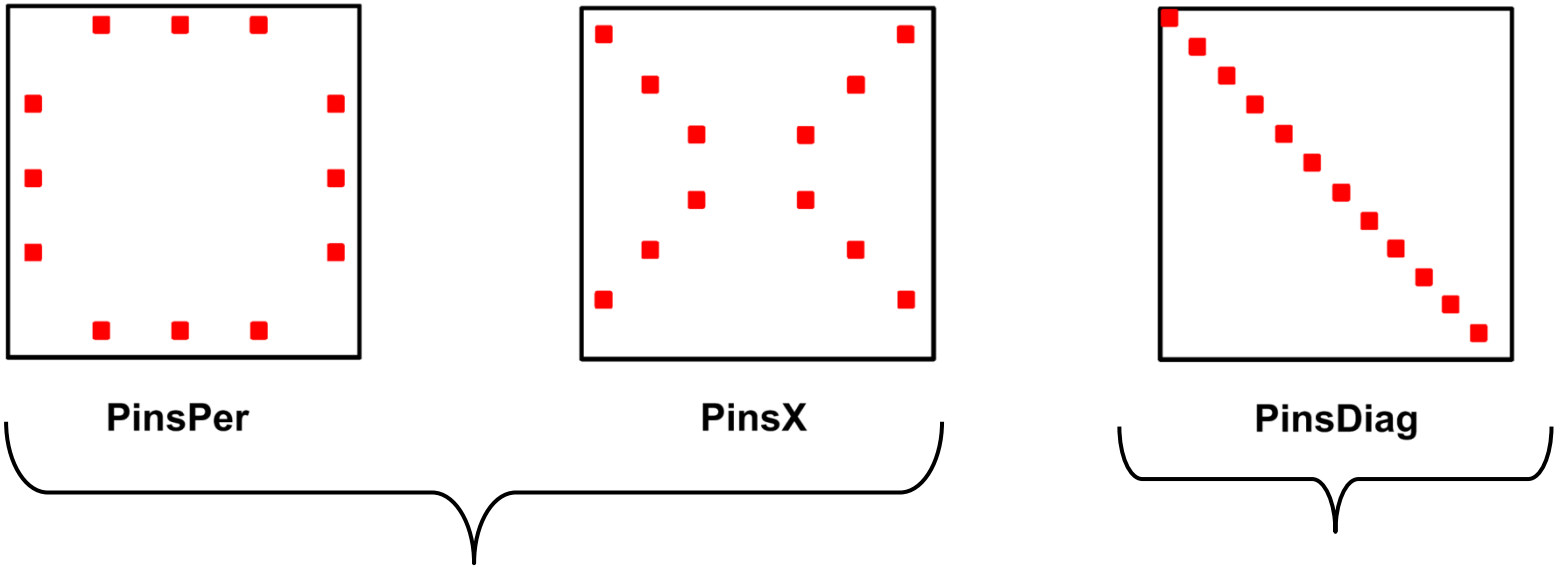
Small Block



- 60% reduction in area and 55% reduction in cost

Logic Block Pin Positions

- Three schemes

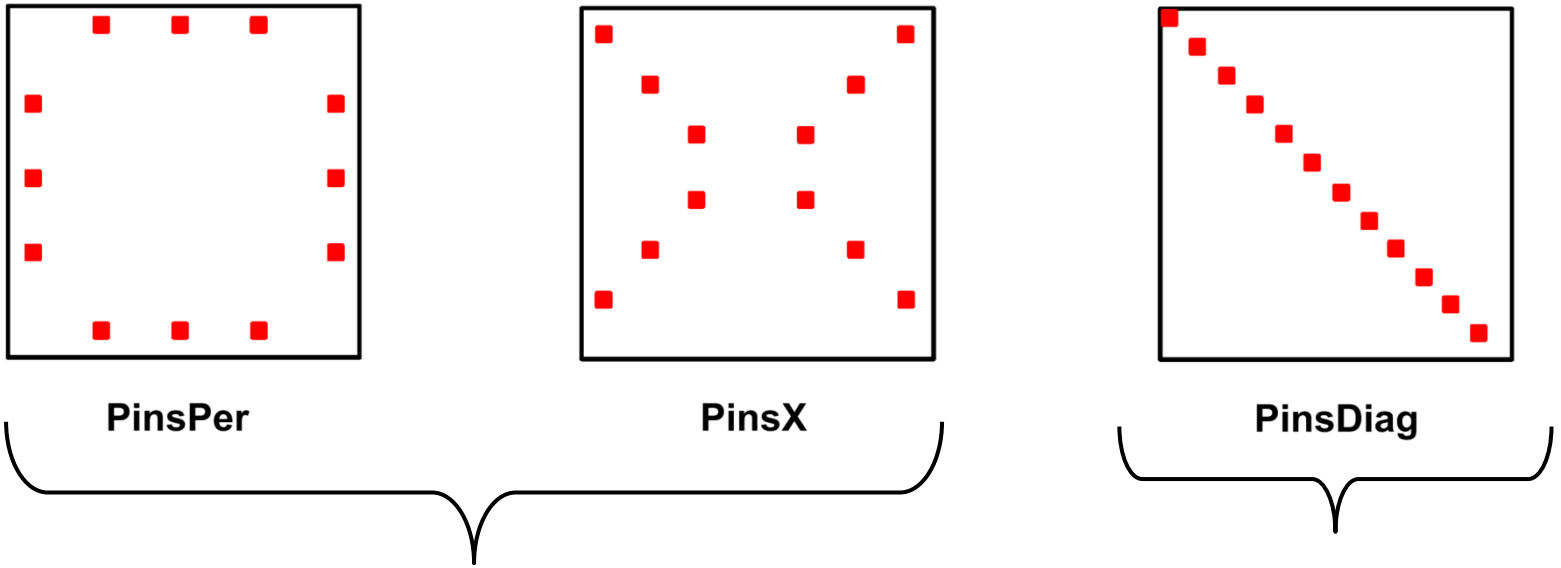


- *Multiple pins per track*
- *More tracks available for routing*
- *Each pin can connect to fewer tracks*

- *Each pin can connect to more tracks*
- *Fewer routing tracks in the lowest layer*

Logic Block Pin Positions

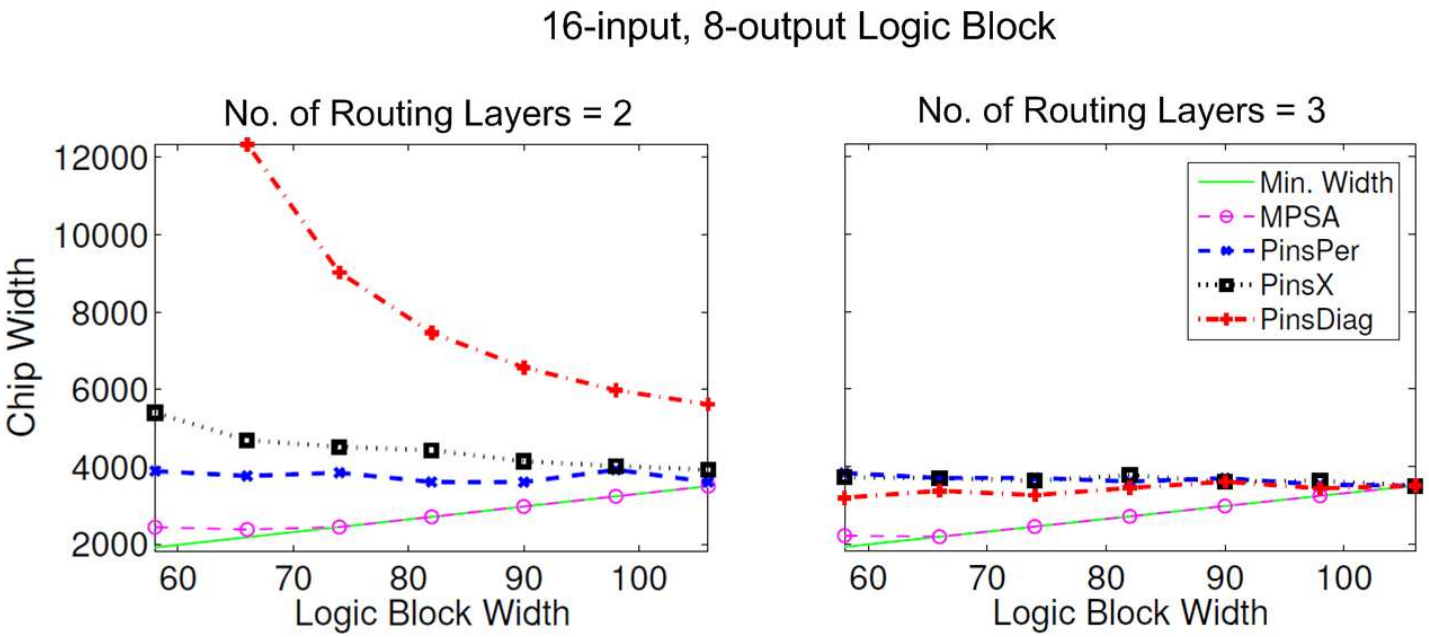
- Three schemes



- *Better when routing resources are limited (e.g., routing layers = 2)*
- *Better when number of routing resources is large*

Experiments used best scheme for each case

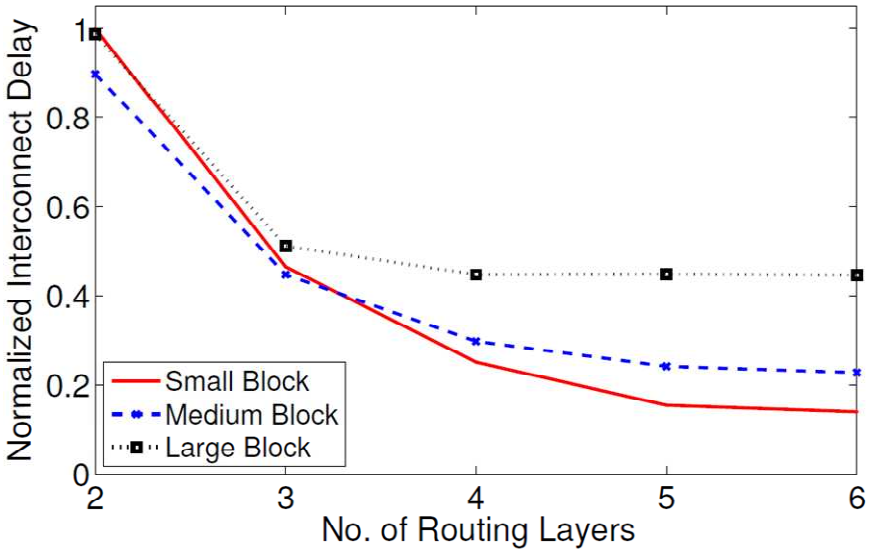
Logic Block Pin Positions

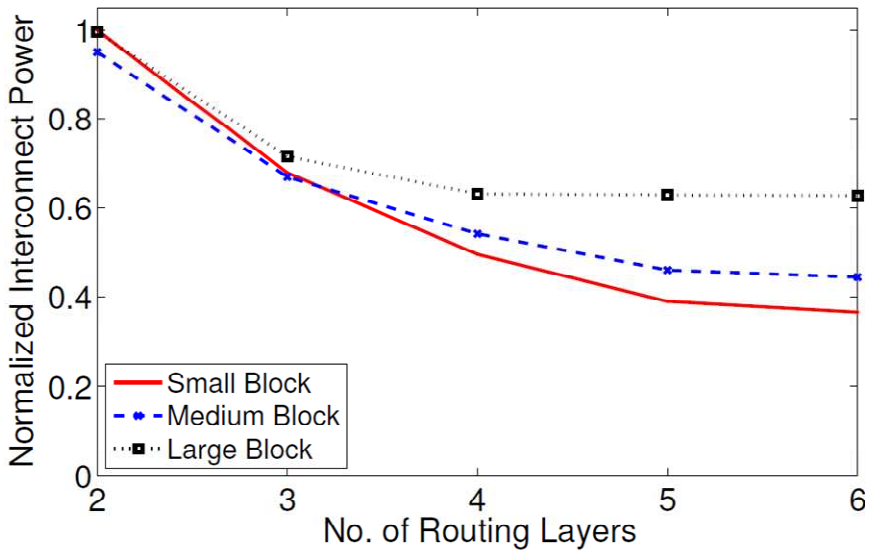


- Significant difference between different schemes
- Performance dependent on
  - Routing fabric architecture
  - Number of routing layers

Trends for Heterogeneous Circuits

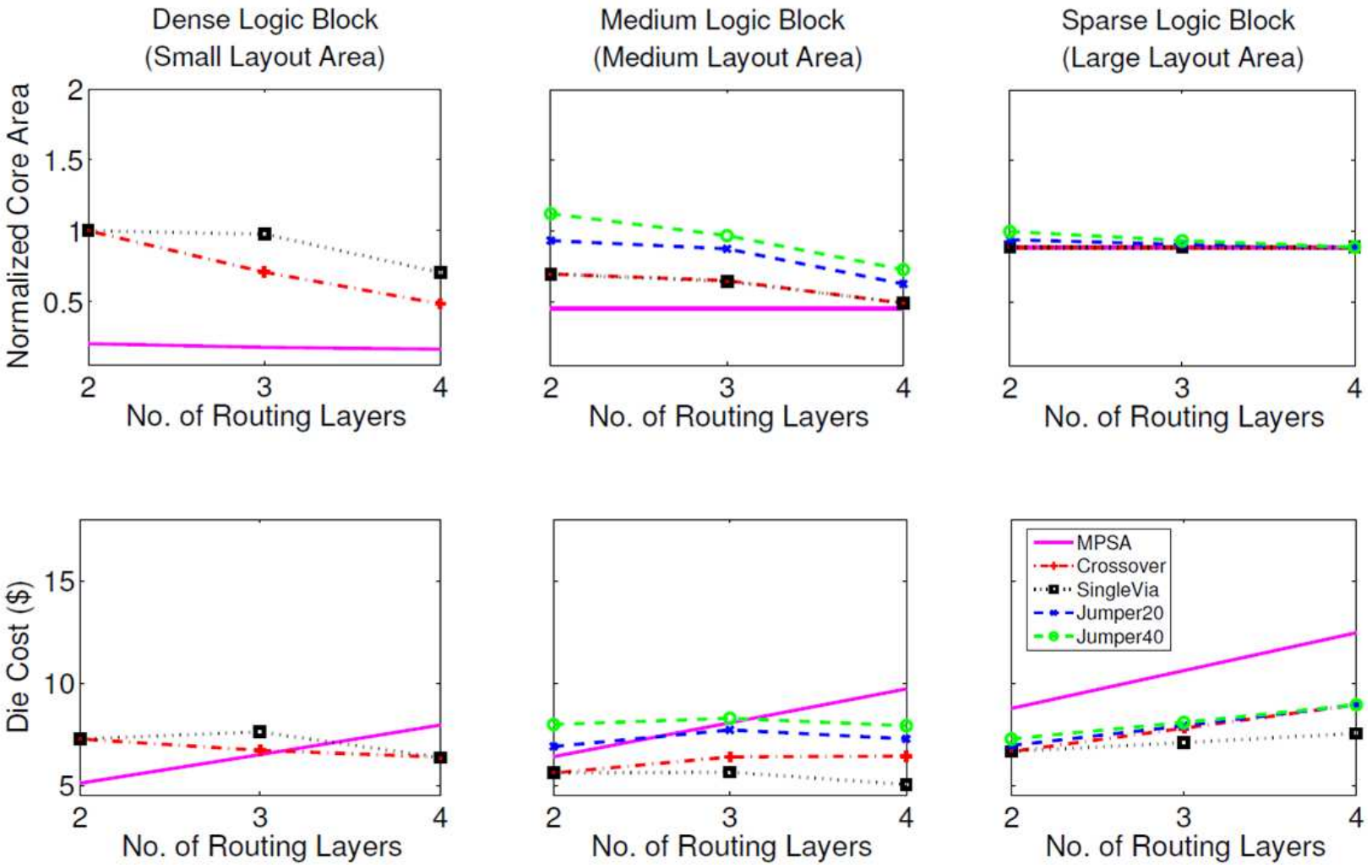
- Delay and Power





  - Best performance obtained with 3 or 4 layers
  - More than 4 layers offer little advantage

VPSA Area and Die-cost Trends



Technology Scaling

Parameter	Relation	Full Scaling	General Scaling	Fixed-Voltage Scaling
W, L, t_{ox}		$1/S$	$1/S$	$1/S$
V_{DD}, V_T		$1/S$	$1/U$	1
N_{SUB}	V/W_{depl}^2	S	S^2/U	S^2
Area/Device	WL	$1/S^2$	$1/S^2$	$1/S^2$
C_{ox}	$1/t_{ox}$	S	S	S
C_{gate}	$C_{ox}WL$	$1/S$	$1/S$	$1/S$
k_n, k_p	$C_{ox}W/L$	S	S	S
I_{sat}	$C_{ox}WV$	$1/S$	$1/U$	1
Current Density	$I_{sat}/Area$	S	S^2/U	S^2
Ron	V/I_{sat}	1	1	1
Intrinsic Delay	$R_{on}C_{gate}$	$1/S$	$1/S$	$1/S$
P	$I_{sat}V$	$1/S^2$	$1/U^2$	1
Power Density	$P/Area$	1	S^2/U^2	S^2