A Fully Integrated 660 MHz Low-Swing Energy-Recycling DC–DC Converter

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***Abstract*—A fully integrated 0.18 μm DC–DC buck converter using a low-swing "stacked driver" configuration is reported in this paper. A high switching frequency of 660 MHz reduces filter components to fit on chip, but this suffers from high switching losses. These losses are reduced using: 1) low-swing drivers; 2) supply stacking; and 3) introducing a charge transfer path to deliver excess charge from the positive metal-oxide semiconductor drive chain to the load, thereby recycling the charge. The working prototype circuit converts 2.2 to 0.75–1.0 V at 40–55 mA. Design and simulation of an improved circuit is also included that further improves the efficiency by enhancing the charge recycling path, providing automated zero voltage switching (ZVS) operation, and synchronizing the half-swing gating signals.**

***Index Terms*—Charge recycling, integrated output filter, low-power stacked driver, subgigahertz switching, switch mode DC–DC converter.**

I. Introduction

POWER consumption of CMOS digital logic designs has increased rapidly for the last several years. It has become an important issue not only in battery-powered applications, but also in high-performance digital designs due to packaging, cooling, and energy costs.

In modern high-performance CMOS processors, dynamic voltage and frequency scaling (DVFS) technique is commonly used to save dynamic power according to (1). This equation is an approximation that is commonly used to model dynamic power dissipation in digital circuits [1]

$$P_{\rm dis} = CV_{DD}^2 f_{\rm clk}. \quad (1)$$

Here, $P_{\rm dis}$, C, V_{DD}, and $f_{\rm clk}$ are the total dynamic power dissipation, total capacitance, supply voltage, and clock frequency, respectively.

Although scaling a common supply voltage may be appropriate for many applications, this degrades overall system performance [2]. Since dynamic power is a quadratic function of voltage, parts of the circuit that are not performance-critical can operate at a reduced supply voltage to save significant energy. This requires an additional ON-chip voltage supply. Another power-saving technique is to employ adaptive body biasing, where additional voltage supplies are used to dynamically adjust transistor threshold voltages between high-performance and low-power modes. Generating these additional supply voltages with an ON-chip power converter rather than OFF-chip can simplify chip and board design and reduce costs.

In integrated power converter designs, smaller inductor and capacitor values are much preferred to save ON-chip area. Converter design formulas indicate that a higher switching frequency reduces the size of the passive components needed. However, operating at a high frequency increases switching losses through the energy dissipated in the power MOSFETs and their gate drivers. Overall, these switching losses are a significant part of the total losses of a dc–dc converter.

In modern switching converters, zero voltage switching (ZVS) is a common technique to reduce dynamic power loss in the power MOSFET transistors [3], but gate driver loss remains significant. The main idea behind ZVS is to turn ON a power transistor only when the voltage drop across the source/drain terminals is 0 V, resulting in no power loss because no current can flow. In [4]–[6], the ZVS concept is applied to a high-frequency clock driver for very large scale integration (VLSI) applications, resulting in the integrated clock driver/power converter circuit shown in Fig. 1. This circuit recovers energy stored in the main clock capacitor $C_{\rm clk}$ by delivering the energy to the load R_L, a concept called *energy recycling*, but this does not attempt to save energy used in the "front-end" gate driver chain.

In this paper, energy-saving techniques are applied to the front-end drive chain and main power transistors of a fully integrated buck converter. Earlier versions of this paper appeared as [7] and [8], where separate chains of inverter gates are used to drive each of the power transistors in the buck converter. The circuit combines low-swing drivers and supply stacking techniques to reduce switching losses of the gate driver chain. In addition, the circuit delivers excess charge from the positive metal-oxide semiconductor (PMOS) drive chain to the load, a form of energy recycling, to improve the overall conversion efficiency.

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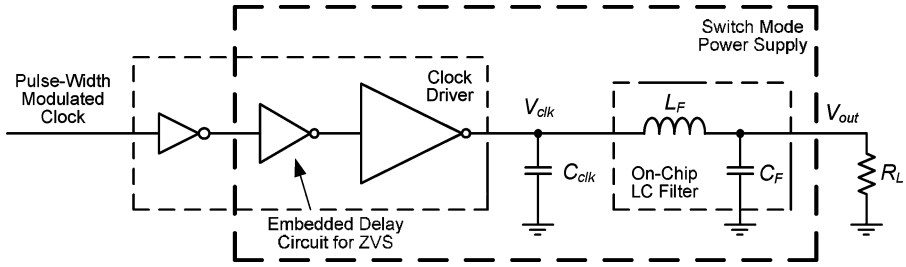

Fig. 1. Recycling clock energy with a dc–dc converter (approximate model).

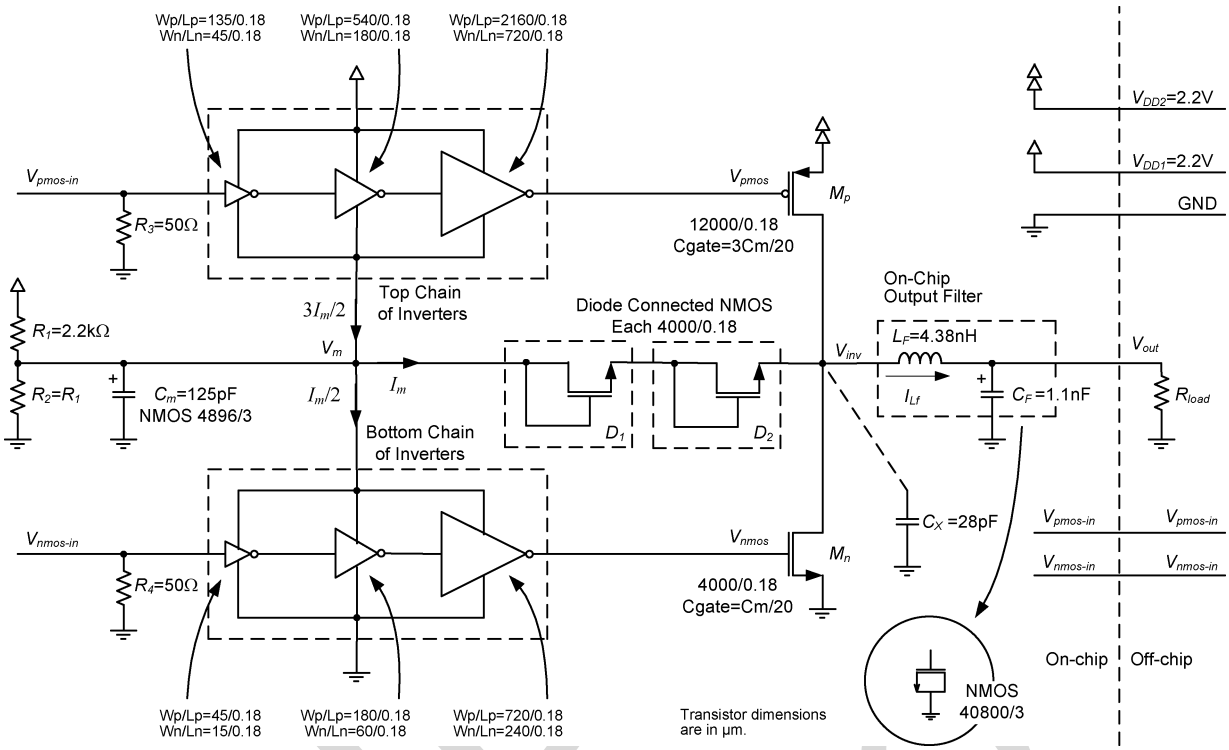

Fig. 2. Circuit diagram of the implemented dc–dc converter prototype with charge-recycling diodes.

The behavior of switching converters below a switching frequency of 2 MHz have been previously investigated in [9] and [10], and converter models were introduced that include the nonlinearities and parasitics. On the other hand, [11] is an example of a fully integrated step-down converter fabricated in a 0.18 μm SiGe RF BiCMOS process. The converter provides a programmable 1.5–2 V output voltage at a 200 mA current rating with a switching frequency of 45 MHz. That design utilizes a two-stage interleaved ZVS synchronous buck topology and has a maximum efficiency of 65%.

This paper improves upon a previous dc–dc converter design by the authors. In [7], a fabricated chip was successfully tested and corresponding simulation and measurement results were reported. In this paper, a new circuit design is simulated to demonstrate improvements to the charge recycling path, ZVS operation, and half-swing gating signal propagation.

This paper is organized as follows. Design ideas are presented in Section II, which also includes idealized timing diagrams and introduces the energy-saving design techniques used. Chip test results are discussed in Section III. Section IV presents improvements based on simulations, and finally, conclusions are made in Section V.

II. Circuit Design

A. Basic Operation

The circuit diagram of the implemented CMOS-based buck converter is shown in Fig. 2. C_x represents all the parasitic capacitances at node $V_{\rm inv}$ including M_p and M_n drain to ground capacitances. When both M_p and M_n are OFF, a positive inductor current will remove charge from C_x, reducing $V_{\rm inv}$, whereas a negative inductor current will charge C_x, increasing $V_{\rm inv}$. When $V_{\rm inv} = 0$, the M_n transistor is turned ON, while when $V_{\rm inv} = V_{DD}$, the M_p transistor is turned ON. In this way, ZVS operation is achieved for both M_n and M_p transistors, respectively. This can be accomplished by independently driving the transistor gates.

B. Energy-Saving Design Techniques

In this design, the following energy-saving design techniques have been employed.

1) The negative metal-oxide semiconductor (NMOS) and PMOS output transistors have large input gate capacitances, requiring them to be driven by a chain of tapered inverters referred to here as the front-end drive chain. Separate drive chains are required to allow precise control of the NMOS and PMOS turn-ON and turn-OFF times to achieve ZVS. Despite ZVS, which reduces energy waste in the final NMOS/PMOS pair, significant losses are associated with operating the two drive chains and the gates of the output transistors at high switching frequencies. To reduce the energy lost at every transition, each drive chain employs low-swing signaling by swinging only half-rail, between 0 and $V_{DD}/2$ or between $V_{DD}/2$ and V_{DD} for NMOS and PMOS, respectively. This saves a significant amount of energy compared to full-rail switching. However, the outputs of the low-swing drive chains must turn ON their respective NMOS and PMOS output transistors sufficiently, so it is essential that $V_{DD}/2$ be well above $V_{\text{t-NMOS}}$ and $|V_{\text{t-PMOS}}|$. Here, $V_{\text{t-NMOS}}$ and $V_{\text{t-PMOS}}$ denote the threshold voltage of NMOS and PMOS transistors, respectively. To increase overdrive, devices with low threshold voltage (low-V_t) may be used for the NMOS and PMOS output transistors as well as the rest of the drive chain.
2) A half-rail swing for both drive chains allows the NMOS and PMOS chains to share the common reference voltage of $V_{DD}/2$. This allows energy reuse in the form of voltage supply stacking as shown in Fig. 2. Charge used by the upper PMOS drive chain still has unused potential, so it can be reused by the lower NMOS drive chain. This technique was also used in [12]. A more general case of supply stacking is called charge recycling in [13].
3) The PMOS output transistor M_p in Fig. 2 is three times wider than NMOS output transistor M_n to give similar output characteristics. As a result, the PMOS drive chain (top inverter chain) is much larger and requires approximately three times as much charge to operate than the NMOS drive chain (bottom inverter chain). Consequently, charge accumulates at node V_m, which is stored in the middle capacitor C_m. The excess charge is *recycled* by delivering it to the converter output load through the two series diode-connected NMOS transistors, D_1 and D_2.

C. Complete Operation

In Fig. 3, the two time periods when both transistors are OFF are characterized as T_{delay1} and T_{delay2}, corresponding to the delay time needed to implement ZVS for the M_n and M_p transistors, respectively. There are four intervals of operation.

1) Interval 1 (time 0 to $D \times T_{\text{sw}}$): M_p is ON. During this time, the inductor current increases linearly since the voltage across it is constant. At the end of this interval, M_p is turned OFF in accordance with the required converter output voltage (the duty cycle).

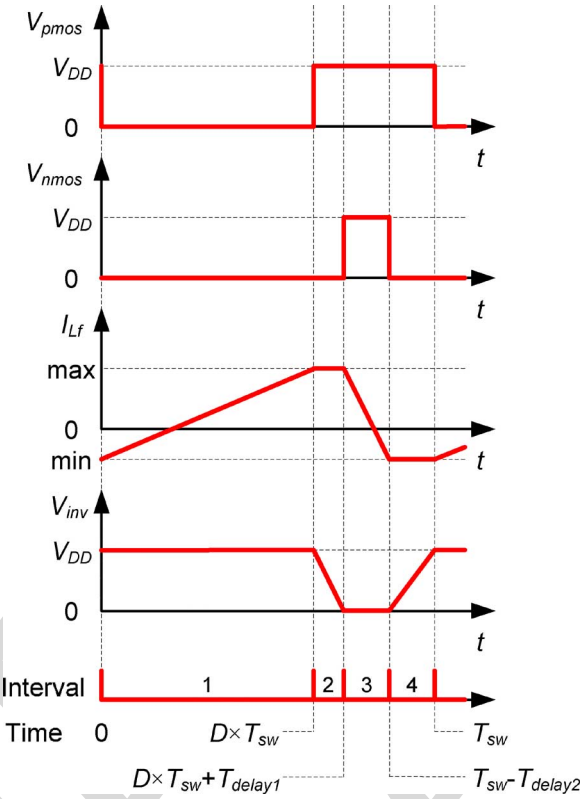

Fig. 3. Idealized timing diagram of the internal signals.

2) Interval 2 (time $D \times T_{\text{sw}}$ to $D \times T_{\text{sw}} + T_{\text{delay1}}$): Both M_p and M_n are OFF. The charge that is stored in the parasitic capacitance C_x is moved to the output circuit through the inductor, as the inductor current cannot be disrupted abruptly. This results in rapid drop of V_{inv}. In this short period of time, the inductor current can be assumed to be constant, as shown.
3) Interval 3 (time $D \times T_{\text{sw}} + T_{\text{delay1}}$ to $T_{\text{sw}} - T_{\text{delay2}}$) starts when the voltage across M_n is close to zero. At this time, the M_n is turned ON under ZVS to provide a low-resistance path for the inductor current. As there is no energy supplied to the system and voltage across the inductor is constant, inductor current decreases linearly and by design reaches some negative value. At this point of time, M_n is turned OFF.
4) Interval 4 (time $T_{\text{sw}} - T_{\text{delay2}}$ to T_{sw}). Both M_p and M_n are OFF. Parasitic capacitance C_x is charged as the inductor current cannot be disrupted abruptly. This results in increase of V_{inv}. At the end of this interval, V_{inv} is close to V_{DD} and M_p is ready to be turned on under ZVS.

Since the size of transistor M_p is set to be three times the size of transistor M_n, and the chain to drive M_p is similarly three times larger than the bottom chain, charge accumulates in the middle capacitor C_m, which should operate near $V_{DD}/2$. In [12], the excess charge is dissipated to ground through an additional regulator forcing node V_m to $V_{DD}/2$. Instead, this paper delivers the extra charge to the converter output circuit to increase efficiency. This task is performed by two series

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diode-connected NMOS transistors, D_1 and D_2. These series diode-connected transistors automatically deliver charge to the load when $V_{\rm inv} < (V_m - 2V_t)$ without a need for additional gating signals. Because the voltage drop across a diode-connected transistor is roughly $V_{DD}/4$, the two diode-connected transistors in series help ensure V_m drops no lower than $V_{DD}/2$ when M_n is ON and $V_{\rm inv}$ is low. Before this voltage is reached, accumulated charge at C_m is removed through the series diode-connected transistors by the inductor L_F in the same manner as L_F is used to perform ZVS by discharging the capacitance C_x. The voltage divider R_1 and R_2 puts V_m near $V_{DD}/2$ at startup and does not significantly contribute to operational power.

Charge recycling occurs during intervals 2 and 4 when both M_p and M_n are OFF and $V_{\rm inv}$ is in transition. In particular, when $V_{\rm inv}$ is rising, there is significant charge stored on the gate of M_p that is discharged through the upper driver to the C_m node at the same time that current is drawn from this node into C_x. When $V_{\rm inv}$ is falling, any additional surplus charge from the top chain of drivers can also be delivered to C_x.

In this design, weak negative feedback helps keep V_m near a stable operating point of $V_{DD}/2$. Since V_m is the supply voltage to the bottom chain, if V_m increases, power drawn by the bottom chain increases, which causes V_m to drop. At the same time, M_n turns ON with a higher $V_{\rm gs}$, and $V_{\rm inv}$ is pulled closer to the ground, giving D_1 and D_2 a higher $V_{\rm gs}$, facilitating charge removal from C_m. Similarly, if V_m decreases, the top chain receives a higher supply voltage, which results in increasing its power intake and causing V_m to increase. Also, a lower V_m causes D_1 and D_2 to receive lower $V_{\rm gs}$, facilitating accumulation of charge in C_m. Capacitance C_m was chosen to be 20 times larger than the NMOS $C_{\rm gate}$ to limit ripple at V_m. Using (2) and (3) from [14] as guidelines and considering maximum $I_{LF} = 2I_{\rm out}$, initial L_F and C_F values were chosen and then optimized using ASITIC parameter extraction tools [15] and circuit simulations. The final design uses L_F and C_F values of 4.38 nH and 1.1 nF, respectively, to operate at a switching frequency of 660 MHz with a voltage ripple of less than 5% at 50 mA load

$$L_F = \frac{DT_{\rm sw}}{2I_{\rm out}}(V_{DD} - V_{\rm out}) \tag{2}$$

$$C_F = \frac{(1-D)}{8(\Delta V_{\rm out,pp}/V_{\rm out})L_F f_{\rm sw}^2}. \tag{3}$$

Here, $T_{\rm sw}$ is the switching period, $f_{\rm sw}$ is the switching frequency, and $\Delta V_{\rm out,pp}/V_{\rm out}$ is the normalized peak-to-peak output voltage ripple.

III. Chip Implementation and Test

A. Chip Implementation

The chip was fabricated in 0.18 μm CMOS. Node V_m, the middle voltage that should remain at $V_{DD}/2$ for supply stacking, is made available OFF-chip to be externally probed or adjusted, if necessary. To keep things simple due to fabrication deadlines, this design does not automatically delay signals to achieve ZVS. Instead, the implementation relies upon the test equipment to generate input signals $V_{\rm pmos\text{-}in}$ and $V_{\rm nmos\text{-}in}$ with the appropriate timing [7].

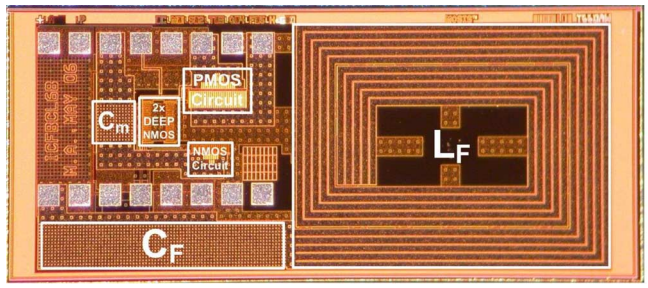

Fig. 4. Chip micrograph.

Ideally, a floating signal generator is needed to drive $V_{\rm pmos\text{-}in}$ with respect to V_m, as the crossover gate voltage for the top inverter chain is about $3V_{DD}/4$. However, a floating signal generator was not available to the authors, and consequently, simulations are done with $V_{\rm pmos\text{-}in}$ driven with respect to ground to keep the conditions in simulations and tests the same. Since the output of a signal generator is not ideal and has rise and fall times, driving $V_{\rm pmos\text{-}in}$ with respect to the system ground would result in a relatively smaller duty ratio be "seen" by that input node (due to the higher crossover voltage). With the odd number of inverters used in the chain, this causes transistor M_p to be ON for a relatively shorter amount of time that reduces the output voltage of the converter. In both simulation and test, manual tuning was performed to obtain ZVS operation.

The chip micrograph is shown in Fig. 4. The 3.4 mm^2 total die area uses 2.5 mm^2 for the converter. Even at 660 MHz, the inductor dominates the area at 1.8 mm^2. Here, the inductor L_F design is two turns of simple concentric coils implemented in the top four metal layers of the chip. A patterned ground shield (PGS) is implemented using the lowest of the six available metal layers [16]–[18]. The current density is 0.122 mA/μm^2. The value of inductance was extracted using ASITIC [15]. Its value was 4.38 nH, at 660 MHz, with lumped "π" model capacitances of 6.5 pF and a Q-factor of 10 at a resonant frequency around 1 GHz. A dc series resistance of 0.7 Ω was also extracted. Although there has been some effort in characterizing magnetic cores at frequencies below 1 MHz [19], the design in this paper uses a coreless inductor, because magnetic cores are not available in conventional CMOS processes, and extra steps are needed to implement them on chip.

B. Chip Test

Testing of this chip was done at $V_{DD} = 2.2$ V. We operate at a higher voltage than the typical 1.8 V for chips fabricated in a 0.18 μm process to emulate the effect of using low-V_t transistors in the design. The CMOS technology we used does not have low-V_t transistors, so our gate drivers and power MOSFETs do not operate as well at 1.8 V. Low-V_t transistors are available in most modern processes.

Conversion efficiency and output voltage measurements are presented in Fig. 5. Ten chips were tested, producing the standard error bars shown in the figure. The physical measurements

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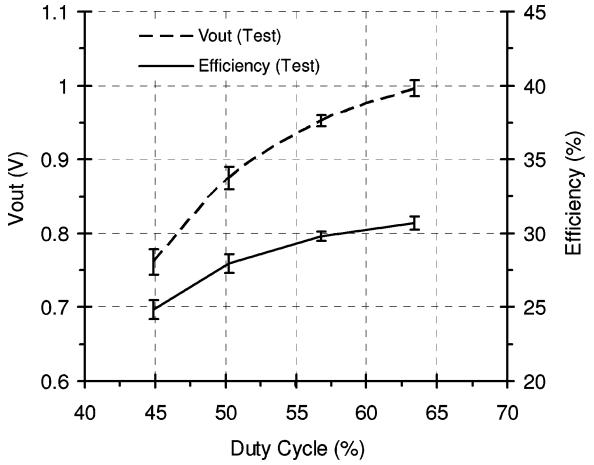

Fig. 5. Measured chip results with standard error (S_E) bars.

required the use of an external supply of 1.1 V connected to V_m because it was higher than the expected voltage of $V_{DD}/2$. However, measurements show that this supply voltage was not delivering any power to the circuit, as it was always sinking current to reduce V_m. The output was adjusted between 0.75 and 1 V by varying duty cycle D from 45% to 64% with a fixed $R_{\rm load} = 18.3\ \Omega$, resulting in output current of 40–55 mA. Conversion efficiency, $P_{\rm out}/P_{\rm in}$, ranges from 25% to 31%. Corresponding simulation results have been previously reported and were discussed in detail by the authors in [7].

IV. Circuit Design Improvements

A. Prototype Limitations

The efficiency of the prototype could be improved in a few ways. First, using transistors with a lower gate-threshold voltage would help the gate drivers have a lower ON-state resistance with the low-swing voltage supply. Similarly, transistors M_p and M_n would also have a lower ON-state resistance, thereby reducing the power dissipation of the circuit. In the design kit used, the standard NMOS and PMOS transistors have threshold voltages of roughly 0.4 and -0.5 V, respectively. When operating at a traditional supply voltage of $V_{DD} = 1.8$ V, the transistor gate voltage for an NMOS transistor could be as high as 1.8 V, ensuring it has a low ON-state resistance. However, in this design, the use of stacked drivers limits the highest gate voltage to 1.1 V. Transistors with a lower threshold voltage, say 0.3 and -0.4 V for NMOS and PMOS, respectively, would turn ON faster and harder. On the other hand, using such low-V_t transistors will increase the OFF-state leakage current through the transistors and contribute to increased static power dissipation of the circuit [1].

Second, power is also lost due to the voltage drop across the series diode-connected transistors D_1 and D_2. These transistors keep the circuit simple, but a more complex circuit could be devised. For example, a circuit in [20] mimics the behavior of a diode using a transistor, where the gate is driven by a voltage comparator sensing V_{DS}. However, any gating circuit used here must operate much more quickly, on the order of tens of picoseconds.

Third, ZVS operation of the circuit was implemented by manually adjusting the input signals. A proper circuit would adjust the ZVS delays dynamically based on the circuit conditions.

B. Improved Circuit Design

To alleviate the shortcomings of the implemented design, a new circuit is proposed as shown in Fig. 6. Regular transistors and a 2.2 V supply are still being used (in simulation), because low-V_t transistors are not available in our 0.18 μm design kit.

1) Improved Charge Recycling Path: In this proposed design, instead of using two series diode-connected NMOS transistors to transfer the excess charge from node V_m to node $V_{\rm inv}$, two series-connected PMOS transistors, $M_{\rm pm1}$ and $M_{\rm pm2}$, are used in a way resembling a logic AND gate. Therefore, when both gating signals are low, these nodes are connected to recycle the excess charge.

Looking at the waveforms of $V_{\rm nmos}$, $V_{\rm pmos}$, and $V_{\rm inv}$ in Fig. 3, with ZVS for M_n, there is a period of time (interval 2) when both M_p and M_n are OFF and $V_{\rm inv}$ is dropping due to the positive current in the inductor L_F. This is the time slot for recycling. Recycling can happen when $V_{\rm nmos}$ is low and $V_{\rm inv} \le V_m$. Recycling cannot happen when $V_{\rm nmos}$ is low and $V_{\rm inv} > V_m$ because no power can flow from V_m to $V_{\rm inv}$. Another way of looking at the recycling circuit is to consider it a second buck converter, consisting of $M_{\rm pm2}$, $M_{\rm pm1}$, and M_n, inside the original converter. This second buck converter would be operational during the later part of the ZVS for M_n dead time, when $V_{\rm inv} \le V_m$.

Fig. 7 shows the slow fall in $V_{\rm inv}$ under ZVS operation of M_n. While $V_{\rm inv} = V_{DD}$, the voltage on V_m is rising due to the $V_{\rm pmos}$ drive current in the top chain of inverters. When $V_{\rm inv}$ is falling, the fall is slowed for a short period when the series PMOS transistors $M_{\rm pm1}$ and $M_{\rm pm2}$ turn ON and C_m and C_x are connected in parallel. During this stage, the voltage V_m is reduced as desired. Once sufficient charge has been removed from C_m, the series PMOS transistors are turned OFF and the fall in $V_{\rm inv}$ proceeds as before. When $V_{\rm inv}$ reaches near 0 V, the NMOS transistor M_n is turned ON. While M_n is ON, $V_{\rm inv}$ might be slightly negative or positive (not shown) due to the direction of the inductor current reversing and the ON-state resistance of the transistor. Afterward, a fast rising edge in $V_{\rm inv}$ is shown, as no ZVS turn-ON delay is employed for the PMOS transistor M_p in Fig. 6.

Signals $V_{\rm nmos}$ and $V_{\rm inv}$ are good candidates to drive $M_{\rm pm1}$ and $M_{\rm pm2}$ transistors, but preliminary simulation results show that a shifted $V_{\rm inv}$ with lower amplitude has a better timing. This leads to the use of $V_{\rm nmos}$ and $V_{\text{inv-shift}}$ as the gating signals. As shown in Fig. 8, $V_{\text{inv-shift}}$ is generated using a simple circuit that resembles a switched capacitor. When $V_{\rm inv} = V_{DD}$, capacitor $C_{\rm shift}$ is charged through diode $D_{\rm shift}$ to $V_{\rm shift} = V_{DD} - (V_m + V_{\rm diode})$. When $V_{\rm inv}$ is dropping, $D_{\rm shift}$ will become reverse-biased and $V_{\text{inv-shift}} = V_{\rm inv} - V_{\rm shift}$. With $V_{DD} = 2.2$ V, $V_m = 1.1$ V, and $V_{\rm diode} \cong 0.6$ V, then $V_{\rm shift} = 0.5$ V is achieved.

Also, the size of $M_{\rm pm2}$ is smaller than $M_{\rm pm1}$ to avoid loading a small chain (the lower chain) with a big PMOS gate. While the ratio of the transistor sizes is not optimal, as long as the sum

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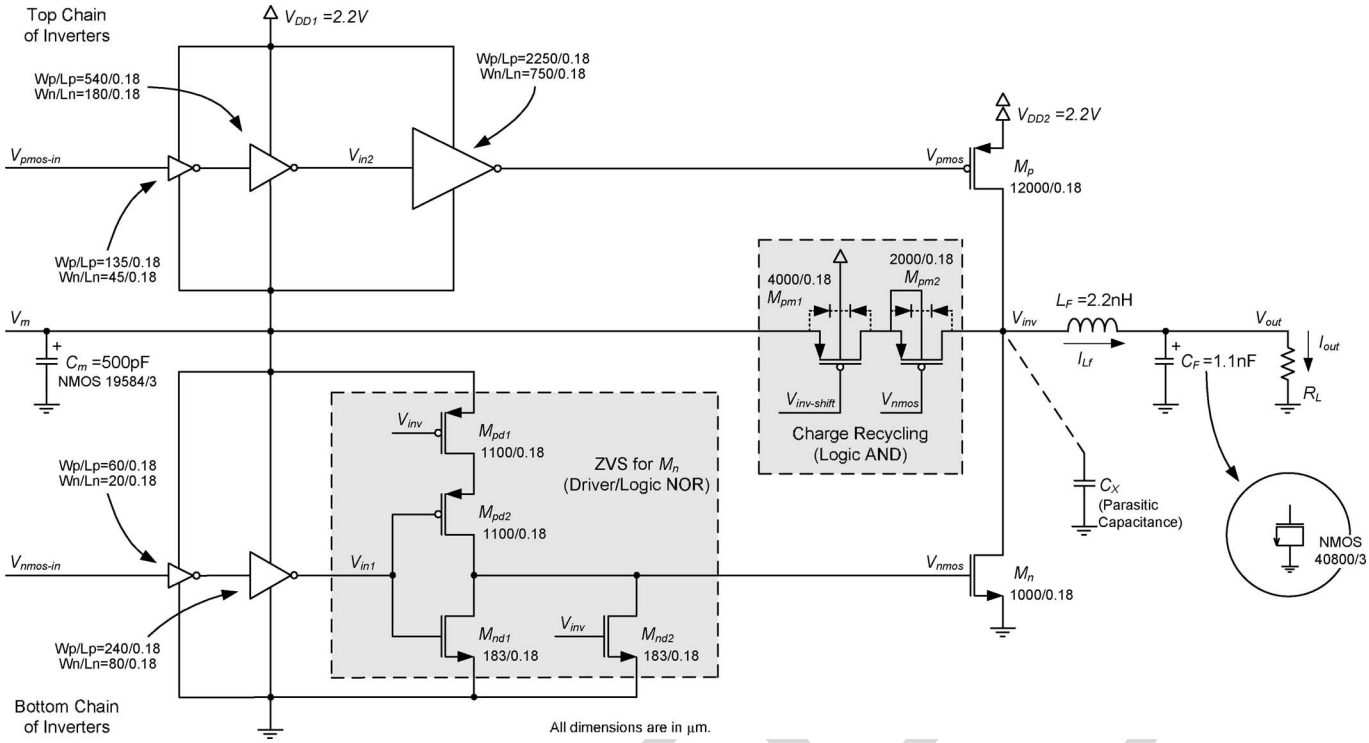

Fig. 6. Circuit diagram of the proposed ZVS and charge-recycling circuits for the dc–dc converter (coupling capacitors C_{c1} and C_{c2} are not shown for clarity).

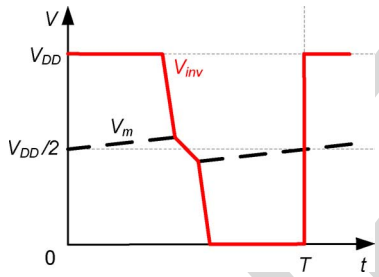

Fig. 7. Idealized timing diagram of the improved circuit diagram (ZVS on one edge only).

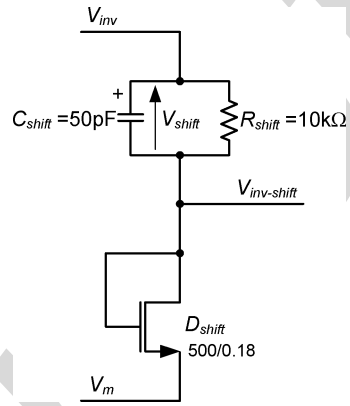

Fig. 8. Generating shifted voltage of $V_{\mathrm{inv\text{-}shift}}$.

of the series resistance is small, power loss in the recycling path will be low.

To disable the intrinsic body diodes, the body of M_{pm1} is connected to V_{DD}, which also increases its absolute threshold voltage value. This is another reason for using of $V_{\mathrm{inv\text{-}shift}}$ rather than V_{inv} as a gating signal. The body of M_{pm2} is connected to its source to keep the threshold voltage intact, but there are periods of time that its body diode is forward-biased. Since M_{pm1} is ON when V_{inv} is low, there would not be any current flowing from V_{inv} to V_m through the (forward biased) body diode of M_{pm2} and the (already turned on) transistor M_{pm1}.

2) Improved ZVS Operation: The effective duty cycle seen by the power circuit depends on various parameters, among which are the value of voltage V_m, the time delay needed to implement ZVS, and the existence of stray resistance, capacitance, and inductance in the actual circuit.

The NMOS ZVS implementation introduced in Fig. 6 is an improved version of the implementation presented by the authors in [4] and [6]. In that design, direct feedback from V_{inv} was used to drive the PMOS transistor that turns ON M_n. Because the gating signal to the NMOS transistor that turns OFF M_n was out of phase with the feedback signal, there could have been a period of time that both the driver PMOS and NMOS transistors are ON. To circumvent this problem, the supply to the lower driver inverter was taken from the V_{pmos} node, which was swinging between V_{DD} and zero.

In the circuit shown in Fig. 6, a complete logic NOR gate is implemented inside the driver inverter chain. This performs ZVS by gating M_{pd1} using V_{inv}. The two NMOS transistors in the logic can have the same size as the original inverter NMOS

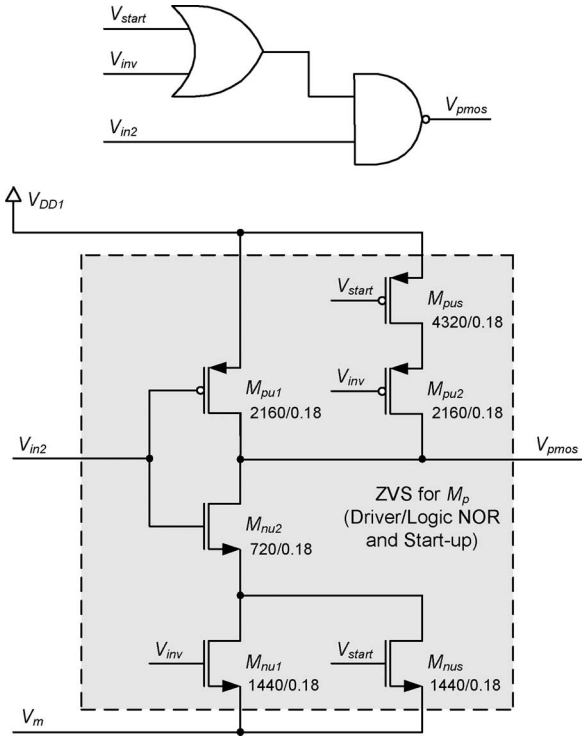

Fig. 9. ZVS logic and circuitry for M_p.

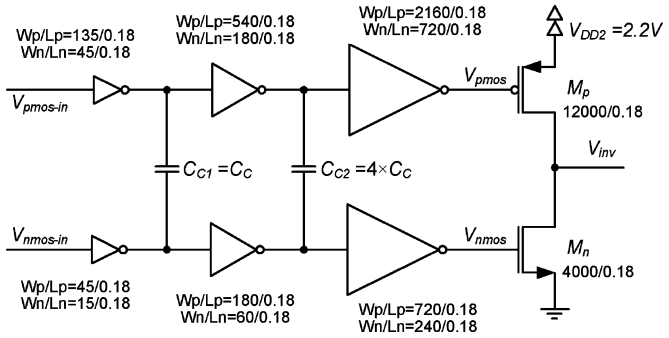

Fig. 10. Use of capacitive coupling to reduce skew.

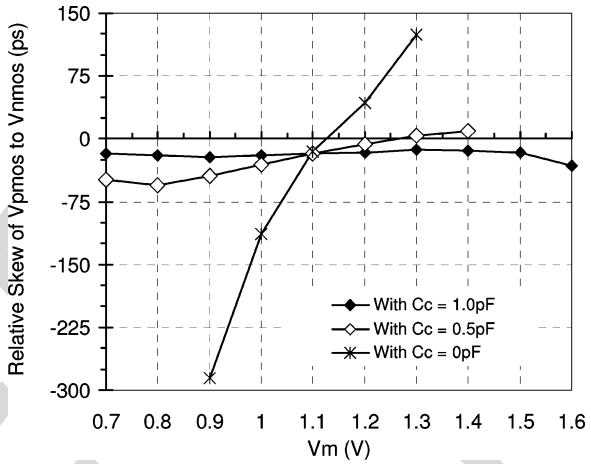

Fig. 11. Simulated effect of C_c on the relative skew of the gating signals.

transistor they replace, but the size of the PMOS transistors should be doubled to keep the drive effort as before.

In Fig. 6, size of the inductor L_F is reduced from 4.38 to 2.2 nH to increase the peak-to-peak value of the current in the inductor. This would increase the built-up current in L_F and facilitates the discharging/charging of C_x.

The ZVS circuit for the PMOS transistor M_p is the dual of the ZVS circuit for the NMOS transistor M_n and is shown in Fig. 9. To implement ZVS for M_p, a negative inductor current is needed. That means for a specific dc output current, a higher peak-to-peak inductor current will be observed; thus, the rms value of the current is increased, which will result in increased resistive losses in the system. On the other hand, ZVS for the PMOS transistor will reduce dynamic losses in the source–drain circuit of M_p and a smaller inductor is required. Thus, ZVS for PMOS may or may not provide a net reduction of power consumption depending on the operating conditions of the system.

It is necessary to disable the M_p ZVS circuitry and charge up C_x when no negative inductor current is present, such as at system start-up. At the start-up, the ZVS circuit must wait for the load voltage to rise so that a negative inductor current can occur to charge up C_x and bring up $V_{\rm inv}$. To detect start-up conditions, $V_{\rm out}$ can be sensed using a voltage comparator to produce the gating signal $V_{\rm start}$, which disables ZVS for M_p and charges C_x at the correct time.

3) Improved Half-Swing Gating Signal Propagation: In this improved design, the ZVS circuitry will automatically recycle charge and delay turning ON M_p or M_n according to conditions at $V_{\rm inv}$. This alleviates the need for external control signals to incorporate the required delays. Instead, control signals $V_{\rm pmos}$ and $V_{\rm nmos}$ should be as closely synchronized as possible. However, voltage supply mismatch caused by variation of V_m or noise in V_{DD} or ground can result in unequal propagation delays through the driver chains, causing $V_{\rm pmos}$ and $V_{\rm nmos}$ to arrive at different times than intended. In general, this condition is referred to as signal skew.

To circumvent skew, capacitive coupling is used to synchronize the signals [21] as shown in Fig. 10. The size of the coupling capacitors is determined such that when the signal in one side of the capacitor is changing, the other side will change as well.

The low-swing circuit of Fig. 10 is simulated with different values of C_c. As shown in Fig. 11, the use of coupling capacitors reduces the time difference between the rising edge of signals $V_{\rm pmos}$ and $V_{\rm nmos}$. Based on the curves in Fig. 11, a value of 1 pF is chosen for C_c, resulting in a short skew of about -20 ps between the two gating signals. However, in this short interval of time, both M_p and M_n are OFF, avoiding any possible short circuit from V_{DD} to the ground. Coupling capacitors $C_{c1} = 1$ pF and $C_{c2} = 4$ pF are also used in Fig. 6, but not shown here for clarity.

C. Simulation of the Improved Circuit

The fully featured circuit is simulated to provide voltage and current waveforms. The simulated circuit is shown in Fig. 6, except transistor sizes are slightly adjusted due to the use of

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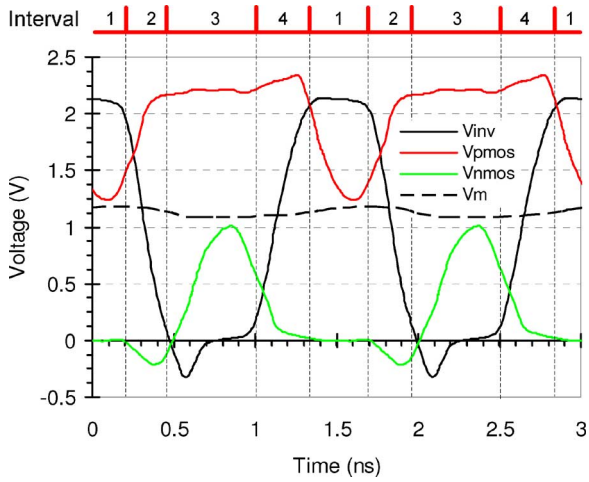

Fig. 12. Simulated voltage waveforms of Fig. 6 with M_p ZVS circuitry of Fig. 9 ($L_F = 1.1$ nH).

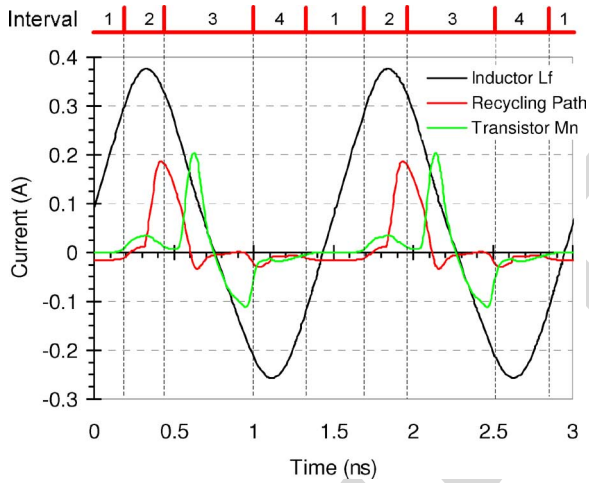

Fig. 13. Simulated current waveforms of Fig. 6 with M_p ZVS circuitry of Fig. 9 ($L_F = 1.1$ nH).

ZVS circuitry for M_p shown in Fig. 9. Simulated waveforms are provided in Figs. 12 and 13 running at $I_{\text{out}} = 50$ mA, $D = 50\%$, and $L_F = 1.1$ nH with ZVS for M_p and M_n. In this simulation, the value of L_F is chosen so that a negative inductor current, which is needed for proper operation of ZVS for M_p, would be provided. At this operating point, $V_m = 1.13$ V, $V_{\text{out}} = 0.95$ V, and $\eta = 38.3\%$. For proper operation of the circuit with ZVS for both M_p and M_n, the duty cycle range is limited between 50% and 60%. As can be observed in Fig. 12, the stacked low-swing driver design results in V_{pmos} swing between V_{DD} and $V_{DD}/2$, and V_{nmos} swing between $V_{DD}/2$ and zero. Also, note that these two gating signals are active at nonoverlapping times due to the ZVS circuitry. Comparing Fig. 12 to Fig. 13, the latter shows idealized voltage waveforms with V_{inv} at a higher than 50% duty cycle.

Fig. 13 shows the reversing inductor current. The current, which contains a net positive dc component, goes negative for the ZVS operation of M_p. Taken together with Fig. 12, which illustrates the delayed rise of V_{nmos} and the delayed fall of V_{pmos}, this result indicates that ZVS operation for M_n and M_p is functioning correctly. In Fig. 13, the current through the recycling path and the current through M_n are out of phase, which indicates that recycled charge is not lost through M_n but it goes through the inductor to the load. In the graphs of Figs. 12 and 13, it should be noted that while the inductor current is smooth, transistor M_n current is not since the current is charging/discharging stray capacitances between the source and drain terminals of M_n.

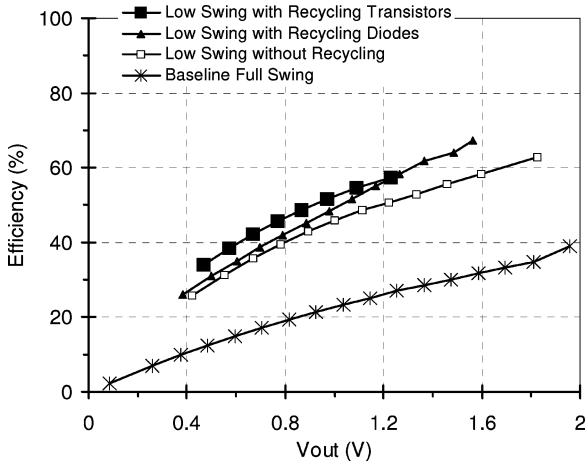

Fig. 14. Simulated efficiency versus output voltage for four variants of Fig. 6 ($L_F = 2.2$ nH).

To evaluate the benefits of driver charge recycling, four variants of the circuit were simulated: 1) baseline converter using two full-swing drivers; 2) low-swing/stacked drive chain is added and only ZVS for M_n is implemented; 3) recycling diode-connected NMOS transistors and C_m are added to 2) to recycle energy; and 4) recycling PMOS transistors and C_m are added to 2) to recycle energy. Only in 2), a supply voltage of $V_{DD}/2$ is connected to node V_m to keep it stable, otherwise V_m would rise. Simulations show that this voltage supply sinks (consumes) about 20 mA of current, which adds to the power consumption of the converter circuit itself.

Simulations of these four circuits are performed at a fixed load current of $I_{\text{out}} = 100$ mA and $L_F = 2.2$ nH, and the results are shown in Figs. 14 and 15. In these simulations, the value of L_F is chosen so that the duty cycle range in which the converter circuit is operational with full swing V_{inv} is increased. As a result, ZVS for M_p is not employed since the inductor current does not reverse. The simulated waveforms were examined individually and data points corresponding to full swing V_{inv} are reported. (V_{inv} is considered to be full swing when its maximum value is above 2.0 V and its minimum value is below 0.2 V.) To make the task of comparing different variants of the circuit at each output voltage (and thus power) level easier, Fig. 14 shows efficiency as a function of output voltage while Fig. 15 shows the output voltage as a function of duty cycle.

As expected, the circuit with all the options 4) has the highest efficiency. Thus, using recycling transistors will improve the

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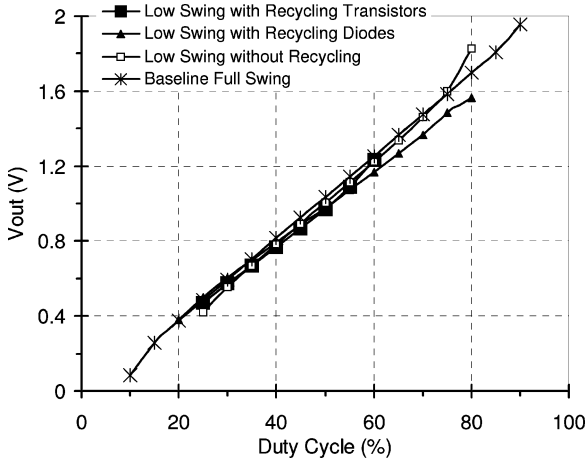

Fig. 15. Simulated output voltage versus duty cycle for four variants of Fig. 6 ($L_F = 2.2$ nH).

TABLE I
POWER CONSUMPTION BREAKDOWN OF FIG. 6 ($L_F = 2.2$ nH)

Component	Power (mW)
Total input power intake (taken from V_{DD1} and V_{DD2})	188
Power circuit intake (taken from V_{DD2})	137
Power circuit consumption (adding up the losses in power circuit components and the output power)	145
Driver circuit power intake (taken from V_{DD1}) (includes top and bottom chains, M_n ZVS circuitry and recycling path transistors M_{pm1} and M_{pm2})	50
Top chain power intake (taken from V_{DD1} with respect to V_m)	21
Bottom chain power intake (taken from V_m) (includes M_n ZVS circuitry)	13
Recycling path PMOS transistors M_{pm1} and M_{pm2} losses	16
Transistor M_p losses	38
Transistor M_n losses (under ZVS operation)	2.5
Capacitor C_F losses	Negligible
Inductor L_F losses	7.5
Output power delivered (to load R_L)	97

efficiency compared to the other variants of the circuit. Also, using low-swing drivers with ZVS for M_n will improve the efficiency compared to the full-swing circuit. The baseline full swing has the worst performance. For example, at an output voltage of 1 V, the efficiency of the circuits are: 1) baseline: 22%; 2) low-swing drivers with ZVS: 46%; 3) low-swing drivers with ZVS and energy recycling diode-connected NMOS transistors: 49%; and 4) low-swing drivers with ZVS and energy recycling PMOS transistors: 52%. Thus, the efficiency improves from 22% to 52% with the energy-saving design methodology of using low-swing drivers with ZVS and energy recycling PMOS transistors. While the ZVS circuitry improves the efficiency of the circuit, the added components to implement ZVS still contribute to the driver losses. Thus, it is important to keep the ZVS timing circuitry neat and simple.

Simulated power consumption of various components of the circuit in Fig. 6, at nominal output current of 100 mA and 50% duty cycle, with $L_F = 2.2$ nH and ZVS for M_p disabled, is shown in Table I. Power circuit components are M_p, M_n, L_F, C_F, and the load. As in other simulations in this paper, an ASITIC [15] extracted model and an NMOS transistor model are used for the inductor L_F and for the capacitor C_F, respectively, which ensures that the parasitic losses of these components are accounted for. For the power circuit, power taken from V_{DD2} is less than power calculated by adding up the output power and losses in the power circuit components, because there is a second path for energy to get into the power circuit and that is through the recycling transistors, confirming the functioning energy recycling. The driver circuit consists of the top and bottom chain of inverters, including M_n ZVS circuitry and recycling path transistors $M_{\rm pm1}$ and $M_{\rm pm2}$. The driver circuit is the biggest single consumer of power with 50 mW, justifying our close attention to this part of the circuit. Power transistor M_p is the second highest with 38 mW and the recycling transistors path is third with 16 mW power consumption. Because of the ZVS operation, the transistor M_n is ON for a shorter period of time, and when ON, it has a lower current level; thus, it consumes only 2.3 mW. In this simulation, the power consumption of the top chain is less than twice the bottom chain. The reasons are that although the size of the top chain is about twice the bottom chain, V_m is higher than $V_{DD}/2$ and the ZVS circuitry consumes some power itself.

The circuit of Fig. 6 is basically a buck converter, with a reversing but effectively continuous current in the inductor. In (4), f_c denotes the corner frequency of the output *LC* filter [14]. Simulation results confirm that the output ripple is around 5% for all variants of the circuit

$$\frac{\Delta V_{\rm out,pp}}{V_{\rm out}} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_{\rm sw}}\right)^2. \tag{4}$$

V. CONCLUSION

The low-swing buck converter design presented here demonstrates the operation of a 660 MHz converter implemented in a 0.18 μm process, including ON-chip passives. The measured efficiency obtained is promising for such a prototype and for such a high switching frequency. However, the most important result is that energy recycling has been shown to be an essential and practical way to reduce energy loss in the front-end drive chain and boost overall conversion efficiency. An improved recycling circuitry was also proposed that further improves the efficiency of the implemented circuit. The lack of low-V_t transistors in the prototype reduced the effectiveness of the energy saving, although some saving is evident. Low-V_t transistors are expected to be increasingly available in standard design kits as the methods employed here become commonplace.

The chip area consumed by the converter is dominated by the inductance even at 660 MHz. The ON-chip inductor in the fabricated circuit was designed for an rms current of 50 mA. This represents a power to area ratio of 50 mW/2.5 mm^2.

Ultimately, the switching frequency has to be increased to reduce the size of the passive components, making ON-chip filter components practical. While this implies more switching losses, the steps presented here to reduce the driver power losses mitigate the adverse effects of a high switching frequency. Consequently, it is expected that such high-frequency designs will become of interest in a wide range of integrated circuit applications. The principles developed here are part of a range of low-energy methods, which will in time allow chips to be powered in an efficient way.

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Dr. Palmer is a Chartered Engineer in the U.K.

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A Fully Integrated 660 MHz Low-Swing Energy-Recycling DC–DC Converter

Mehdi Alimadadi, Samad Sheikhaei, *Student Member, IEEE*, Guy Lemieux, *Senior Member, IEEE*, Shahriar Mirabbasi, *Member, IEEE*, William G. Dunford, *Senior Member, IEEE*, and Patrick R. Palmer, *Member, IEEE*

***Abstract*—A fully integrated 0.18 μm DC–DC buck converter using a low-swing "stacked driver" configuration is reported in this paper. A high switching frequency of 660 MHz reduces filter components to fit on chip, but this suffers from high switching losses. These losses are reduced using: 1) low-swing drivers; 2) supply stacking; and 3) introducing a charge transfer path to deliver excess charge from the positive metal-oxide semiconductor drive chain to the load, thereby recycling the charge. The working prototype circuit converts 2.2 to 0.75–1.0 V at 40–55 mA. Design and simulation of an improved circuit is also included that further improves the efficiency by enhancing the charge recycling path, providing automated zero voltage switching (ZVS) operation, and synchronizing the half-swing gating signals.**

***Index Terms*—Charge recycling, integrated output filter, low-power stacked driver, subgigahertz switching, switch mode DC–DC converter.**

I. Introduction

POWER consumption of CMOS digital logic designs has increased rapidly for the last several years. It has become an important issue not only in battery-powered applications, but also in high-performance digital designs due to packaging, cooling, and energy costs.

In modern high-performance CMOS processors, dynamic voltage and frequency scaling (DVFS) technique is commonly used to save dynamic power according to (1). This equation is an approximation that is commonly used to model dynamic power dissipation in digital circuits [1]

$$P_{\rm dis} = CV_{DD}^2 f_{\rm clk}. \quad (1)$$

Here, $P_{\rm dis}$, C, V_{DD}, and $f_{\rm clk}$ are the total dynamic power dissipation, total capacitance, supply voltage, and clock frequency, respectively.

Although scaling a common supply voltage may be appropriate for many applications, this degrades overall system performance [2]. Since dynamic power is a quadratic function of voltage, parts of the circuit that are not performance-critical can operate at a reduced supply voltage to save significant energy. This requires an additional ON-chip voltage supply. Another power-saving technique is to employ adaptive body biasing, where additional voltage supplies are used to dynamically adjust transistor threshold voltages between high-performance and low-power modes. Generating these additional supply voltages with an ON-chip power converter rather than OFF-chip can simplify chip and board design and reduce costs.

In integrated power converter designs, smaller inductor and capacitor values are much preferred to save ON-chip area. Converter design formulas indicate that a higher switching frequency reduces the size of the passive components needed. However, operating at a high frequency increases switching losses through the energy dissipated in the power MOSFETs and their gate drivers. Overall, these switching losses are a significant part of the total losses of a dc–dc converter.

In modern switching converters, zero voltage switching (ZVS) is a common technique to reduce dynamic power loss in the power MOSFET transistors [3], but gate driver loss remains significant. The main idea behind ZVS is to turn ON a power transistor only when the voltage drop across the source/drain terminals is 0 V, resulting in no power loss because no current can flow. In [4]–[6], the ZVS concept is applied to a high-frequency clock driver for very large scale integration (VLSI) applications, resulting in the integrated clock driver/power converter circuit shown in Fig. 1. This circuit recovers energy stored in the main clock capacitor $C_{\rm clk}$ by delivering the energy to the load R_L, a concept called *energy recycling*, but this does not attempt to save energy used in the "front-end" gate driver chain.

In this paper, energy-saving techniques are applied to the front-end drive chain and main power transistors of a fully integrated buck converter. Earlier versions of this paper appeared as [7] and [8], where separate chains of inverter gates are used to drive each of the power transistors in the buck converter. The circuit combines low-swing drivers and supply stacking techniques to reduce switching losses of the gate driver chain. In addition, the circuit delivers excess charge from the positive metal-oxide semiconductor (PMOS) drive chain to the load, a form of energy recycling, to improve the overall conversion efficiency.

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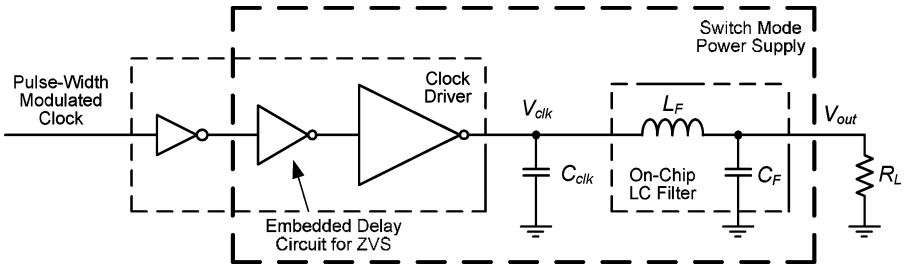

Fig. 1. Recycling clock energy with a dc–dc converter (approximate model).

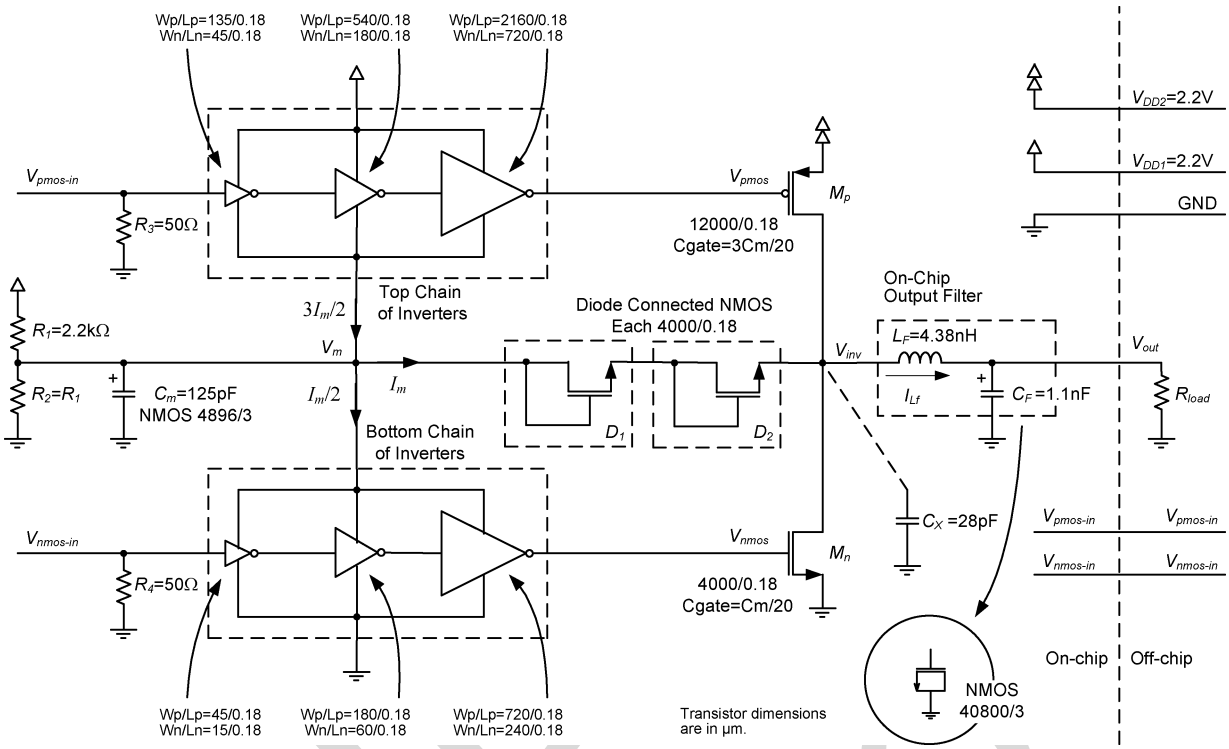

Fig. 2. Circuit diagram of the implemented dc–dc converter prototype with charge-recycling diodes.

The behavior of switching converters below a switching frequency of 2 MHz have been previously investigated in [9] and [10], and converter models were introduced that include the nonlinearities and parasitics. On the other hand, [11] is an example of a fully integrated step-down converter fabricated in a 0.18 μm SiGe RF BiCMOS process. The converter provides a programmable 1.5–2 V output voltage at a 200 mA current rating with a switching frequency of 45 MHz. That design utilizes a two-stage interleaved ZVS synchronous buck topology and has a maximum efficiency of 65%.

This paper improves upon a previous dc–dc converter design by the authors. In [7], a fabricated chip was successfully tested and corresponding simulation and measurement results were reported. In this paper, a new circuit design is simulated to demonstrate improvements to the charge recycling path, ZVS operation, and half-swing gating signal propagation.

This paper is organized as follows. Design ideas are presented in Section II, which also includes idealized timing diagrams and introduces the energy-saving design techniques used. Chip test results are discussed in Section III. Section IV presents improvements based on simulations, and finally, conclusions are made in Section V.

II. Circuit Design

A. Basic Operation

The circuit diagram of the implemented CMOS-based buck converter is shown in Fig. 2. C_x represents all the parasitic capacitances at node $V_{\rm inv}$ including M_p and M_n drain to ground capacitances. When both M_p and M_n are OFF, a positive inductor current will remove charge from C_x, reducing $V_{\rm inv}$, whereas a negative inductor current will charge C_x, increasing $V_{\rm inv}$. When $V_{\rm inv} = 0$, the M_n transistor is turned ON, while when $V_{\rm inv} = V_{DD}$, the M_p transistor is turned ON. In this way, ZVS operation is achieved for both M_n and M_p transistors, respectively. This can be accomplished by independently driving the transistor gates.

B. Energy-Saving Design Techniques

In this design, the following energy-saving design techniques have been employed.

1) The negative metal-oxide semiconductor (NMOS) and PMOS output transistors have large input gate capacitances, requiring them to be driven by a chain of tapered inverters referred to here as the front-end drive chain. Separate drive chains are required to allow precise control of the NMOS and PMOS turn-ON and turn-OFF times to achieve ZVS. Despite ZVS, which reduces energy waste in the final NMOS/PMOS pair, significant losses are associated with operating the two drive chains and the gates of the output transistors at high switching frequencies. To reduce the energy lost at every transition, each drive chain employs low-swing signaling by swinging only half-rail, between 0 and $V_{DD}/2$ or between $V_{DD}/2$ and V_{DD} for NMOS and PMOS, respectively. This saves a significant amount of energy compared to full-rail switching. However, the outputs of the low-swing drive chains must turn ON their respective NMOS and PMOS output transistors sufficiently, so it is essential that $V_{DD}/2$ be well above $V_{\text{t-NMOS}}$ and $|V_{\text{t-PMOS}}|$. Here, $V_{\text{t-NMOS}}$ and $V_{\text{t-PMOS}}$ denote the threshold voltage of NMOS and PMOS transistors, respectively. To increase overdrive, devices with low threshold voltage (low-V_t) may be used for the NMOS and PMOS output transistors as well as the rest of the drive chain.
2) A half-rail swing for both drive chains allows the NMOS and PMOS chains to share the common reference voltage of $V_{DD}/2$. This allows energy reuse in the form of voltage supply stacking as shown in Fig. 2. Charge used by the upper PMOS drive chain still has unused potential, so it can be reused by the lower NMOS drive chain. This technique was also used in [12]. A more general case of supply stacking is called charge recycling in [13].
3) The PMOS output transistor M_p in Fig. 2 is three times wider than NMOS output transistor M_n to give similar output characteristics. As a result, the PMOS drive chain (top inverter chain) is much larger and requires approximately three times as much charge to operate than the NMOS drive chain (bottom inverter chain). Consequently, charge accumulates at node V_m, which is stored in the middle capacitor C_m. The excess charge is *recycled* by delivering it to the converter output load through the two series diode-connected NMOS transistors, D_1 and D_2.

C. Complete Operation

In Fig. 3, the two time periods when both transistors are OFF are characterized as T_{delay1} and T_{delay2}, corresponding to the delay time needed to implement ZVS for the M_n and M_p transistors, respectively. There are four intervals of operation.

1) Interval 1 (time 0 to $D \times T_{\text{sw}}$): M_p is ON. During this time, the inductor current increases linearly since the voltage across it is constant. At the end of this interval, M_p is turned OFF in accordance with the required converter output voltage (the duty cycle).

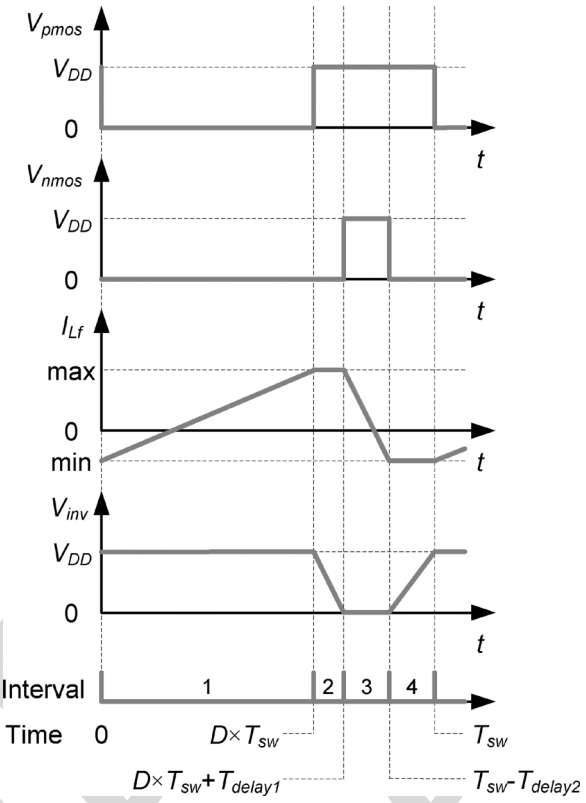

Fig. 3. Idealized timing diagram of the internal signals.

2) Interval 2 (time $D \times T_{\text{sw}}$ to $D \times T_{\text{sw}} + T_{\text{delay1}}$): Both M_p and M_n are OFF. The charge that is stored in the parasitic capacitance C_x is moved to the output circuit through the inductor, as the inductor current cannot be disrupted abruptly. This results in rapid drop of V_{inv}. In this short period of time, the inductor current can be assumed to be constant, as shown.
3) Interval 3 (time $D \times T_{\text{sw}} + T_{\text{delay1}}$ to $T_{\text{sw}} - T_{\text{delay2}}$) starts when the voltage across M_n is close to zero. At this time, the M_n is turned ON under ZVS to provide a low-resistance path for the inductor current. As there is no energy supplied to the system and voltage across the inductor is constant, inductor current decreases linearly and by design reaches some negative value. At this point of time, M_n is turned OFF.
4) Interval 4 (time $T_{\text{sw}} - T_{\text{delay2}}$ to T_{sw}). Both M_p and M_n are OFF. Parasitic capacitance C_x is charged as the inductor current cannot be disrupted abruptly. This results in increase of V_{inv}. At the end of this interval, V_{inv} is close to V_{DD} and M_p is ready to be turned on under ZVS.

Since the size of transistor M_p is set to be three times the size of transistor M_n, and the chain to drive M_p is similarly three times larger than the bottom chain, charge accumulates in the middle capacitor C_m, which should operate near $V_{DD}/2$. In [12], the excess charge is dissipated to ground through an additional regulator forcing node V_m to $V_{DD}/2$. Instead, this paper delivers the extra charge to the converter output circuit to increase efficiency. This task is performed by two series

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diode-connected NMOS transistors, D_1 and D_2. These series diode-connected transistors automatically deliver charge to the load when $V_{\rm inv} < (V_m - 2V_t)$ without a need for additional gating signals. Because the voltage drop across a diode-connected transistor is roughly $V_{DD}/4$, the two diode-connected transistors in series help ensure V_m drops no lower than $V_{DD}/2$ when M_n is ON and $V_{\rm inv}$ is low. Before this voltage is reached, accumulated charge at C_m is removed through the series diode-connected transistors by the inductor L_F in the same manner as L_F is used to perform ZVS by discharging the capacitance C_x. The voltage divider R_1 and R_2 puts V_m near $V_{DD}/2$ at startup and does not significantly contribute to operational power.

Charge recycling occurs during intervals 2 and 4 when both M_p and M_n are OFF and $V_{\rm inv}$ is in transition. In particular, when $V_{\rm inv}$ is rising, there is significant charge stored on the gate of M_p that is discharged through the upper driver to the C_m node at the same time that current is drawn from this node into C_x. When $V_{\rm inv}$ is falling, any additional surplus charge from the top chain of drivers can also be delivered to C_x.

In this design, weak negative feedback helps keep V_m near a stable operating point of $V_{DD}/2$. Since V_m is the supply voltage to the bottom chain, if V_m increases, power drawn by the bottom chain increases, which causes V_m to drop. At the same time, M_n turns ON with a higher $V_{\rm gs}$, and $V_{\rm inv}$ is pulled closer to the ground, giving D_1 and D_2 a higher $V_{\rm gs}$, facilitating charge removal from C_m. Similarly, if V_m decreases, the top chain receives a higher supply voltage, which results in increasing its power intake and causing V_m to increase. Also, a lower V_m causes D_1 and D_2 to receive lower $V_{\rm gs}$, facilitating accumulation of charge in C_m. Capacitance C_m was chosen to be 20 times larger than the NMOS $C_{\rm gate}$ to limit ripple at V_m. Using (2) and (3) from [14] as guidelines and considering maximum $I_{LF} = 2I_{\rm out}$, initial L_F and C_F values were chosen and then optimized using ASITIC parameter extraction tools [15] and circuit simulations. The final design uses L_F and C_F values of 4.38 nH and 1.1 nF, respectively, to operate at a switching frequency of 660 MHz with a voltage ripple of less than 5% at 50 mA load

$$L_F = \frac{DT_{\rm sw}}{2I_{\rm out}}(V_{DD} - V_{\rm out}) \tag{2}$$

$$C_F = \frac{(1-D)}{8(\Delta V_{\rm out,pp}/V_{\rm out})L_F f_{\rm sw}^2}. \tag{3}$$

Here, $T_{\rm sw}$ is the switching period, $f_{\rm sw}$ is the switching frequency, and $\Delta V_{\rm out,pp}/V_{\rm out}$ is the normalized peak-to-peak output voltage ripple.

III. Chip Implementation and Test

A. Chip Implementation

The chip was fabricated in 0.18 μm CMOS. Node V_m, the middle voltage that should remain at $V_{DD}/2$ for supply stacking, is made available OFF-chip to be externally probed or adjusted, if necessary. To keep things simple due to fabrication deadlines, this design does not automatically delay signals to achieve ZVS. Instead, the implementation relies upon the test equipment to generate input signals $V_{\rm pmos\text{-}in}$ and $V_{\rm nmos\text{-}in}$ with the appropriate timing [7].

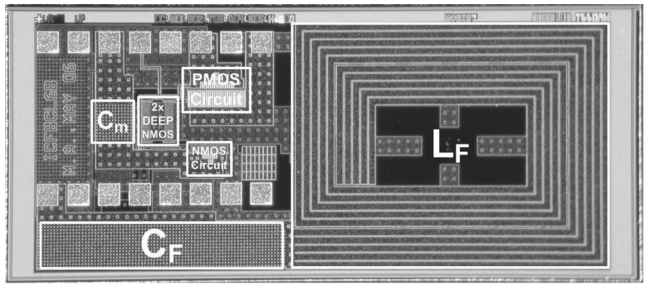

Fig. 4. Chip micrograph.

Ideally, a floating signal generator is needed to drive $V_{\rm pmos\text{-}in}$ with respect to V_m, as the crossover gate voltage for the top inverter chain is about $3V_{DD}/4$. However, a floating signal generator was not available to the authors, and consequently, simulations are done with $V_{\rm pmos\text{-}in}$ driven with respect to ground to keep the conditions in simulations and tests the same. Since the output of a signal generator is not ideal and has rise and fall times, driving $V_{\rm pmos\text{-}in}$ with respect to the system ground would result in a relatively smaller duty ratio be "seen" by that input node (due to the higher crossover voltage). With the odd number of inverters used in the chain, this causes transistor M_p to be ON for a relatively shorter amount of time that reduces the output voltage of the converter. In both simulation and test, manual tuning was performed to obtain ZVS operation.

The chip micrograph is shown in Fig. 4. The 3.4 mm^2 total die area uses 2.5 mm^2 for the converter. Even at 660 MHz, the inductor dominates the area at 1.8 mm^2. Here, the inductor L_F design is two turns of simple concentric coils implemented in the top four metal layers of the chip. A patterned ground shield (PGS) is implemented using the lowest of the six available metal layers [16]–[18]. The current density is 0.122 mA/μm^2. The value of inductance was extracted using ASITIC [15]. Its value was 4.38 nH, at 660 MHz, with lumped "π" model capacitances of 6.5 pF and a Q-factor of 10 at a resonant frequency around 1 GHz. A dc series resistance of 0.7 Ω was also extracted. Although there has been some effort in characterizing magnetic cores at frequencies below 1 MHz [19], the design in this paper uses a coreless inductor, because magnetic cores are not available in conventional CMOS processes, and extra steps are needed to implement them on chip.

B. Chip Test

Testing of this chip was done at $V_{DD} = 2.2$ V. We operate at a higher voltage than the typical 1.8 V for chips fabricated in a 0.18 μm process to emulate the effect of using low-V_t transistors in the design. The CMOS technology we used does not have low-V_t transistors, so our gate drivers and power MOSFETs do not operate as well at 1.8 V. Low-V_t transistors are available in most modern processes.

Conversion efficiency and output voltage measurements are presented in Fig. 5. Ten chips were tested, producing the standard error bars shown in the figure. The physical measurements

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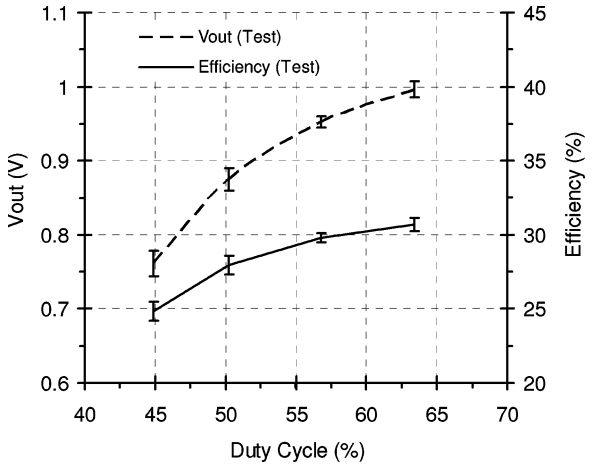

Fig. 5. Measured chip results with standard error (S_E) bars.

required the use of an external supply of 1.1 V connected to V_m because it was higher than the expected voltage of $V_{DD}/2$. However, measurements show that this supply voltage was not delivering any power to the circuit, as it was always sinking current to reduce V_m. The output was adjusted between 0.75 and 1 V by varying duty cycle D from 45% to 64% with a fixed $R_{\rm load} = 18.3\ \Omega$, resulting in output current of 40–55 mA. Conversion efficiency, $P_{\rm out}/P_{\rm in}$, ranges from 25% to 31%. Corresponding simulation results have been previously reported and were discussed in detail by the authors in [7].

IV. Circuit Design Improvements

A. Prototype Limitations

The efficiency of the prototype could be improved in a few ways. First, using transistors with a lower gate-threshold voltage would help the gate drivers have a lower ON-state resistance with the low-swing voltage supply. Similarly, transistors M_p and M_n would also have a lower ON-state resistance, thereby reducing the power dissipation of the circuit. In the design kit used, the standard NMOS and PMOS transistors have threshold voltages of roughly 0.4 and -0.5 V, respectively. When operating at a traditional supply voltage of $V_{DD} = 1.8$ V, the transistor gate voltage for an NMOS transistor could be as high as 1.8 V, ensuring it has a low ON-state resistance. However, in this design, the use of stacked drivers limits the highest gate voltage to 1.1 V. Transistors with a lower threshold voltage, say 0.3 and -0.4 V for NMOS and PMOS, respectively, would turn ON faster and harder. On the other hand, using such low-V_t transistors will increase the OFF-state leakage current through the transistors and contribute to increased static power dissipation of the circuit [1].

Second, power is also lost due to the voltage drop across the series diode-connected transistors D_1 and D_2. These transistors keep the circuit simple, but a more complex circuit could be devised. For example, a circuit in [20] mimics the behavior of a diode using a transistor, where the gate is driven by a voltage comparator sensing V_{DS}. However, any gating circuit used here must operate much more quickly, on the order of tens of picoseconds.

Third, ZVS operation of the circuit was implemented by manually adjusting the input signals. A proper circuit would adjust the ZVS delays dynamically based on the circuit conditions.

B. Improved Circuit Design

To alleviate the shortcomings of the implemented design, a new circuit is proposed as shown in Fig. 6. Regular transistors and a 2.2 V supply are still being used (in simulation), because low-V_t transistors are not available in our 0.18 μm design kit.

1) Improved Charge Recycling Path: In this proposed design, instead of using two series diode-connected NMOS transistors to transfer the excess charge from node V_m to node $V_{\rm inv}$, two series-connected PMOS transistors, $M_{\rm pm1}$ and $M_{\rm pm2}$, are used in a way resembling a logic AND gate. Therefore, when both gating signals are low, these nodes are connected to recycle the excess charge.

Looking at the waveforms of $V_{\rm nmos}$, $V_{\rm pmos}$, and $V_{\rm inv}$ in Fig. 3, with ZVS for M_n, there is a period of time (interval 2) when both M_p and M_n are OFF and $V_{\rm inv}$ is dropping due to the positive current in the inductor L_F. This is the time slot for recycling. Recycling can happen when $V_{\rm nmos}$ is low and $V_{\rm inv} \le V_m$. Recycling cannot happen when $V_{\rm nmos}$ is low and $V_{\rm inv} > V_m$ because no power can flow from V_m to $V_{\rm inv}$. Another way of looking at the recycling circuit is to consider it a second buck converter, consisting of $M_{\rm pm2}$, $M_{\rm pm1}$, and M_n, inside the original converter. This second buck converter would be operational during the later part of the ZVS for M_n dead time, when $V_{\rm inv} \le V_m$.

Fig. 7 shows the slow fall in $V_{\rm inv}$ under ZVS operation of M_n. While $V_{\rm inv} = V_{DD}$, the voltage on V_m is rising due to the $V_{\rm pmos}$ drive current in the top chain of inverters. When $V_{\rm inv}$ is falling, the fall is slowed for a short period when the series PMOS transistors $M_{\rm pm1}$ and $M_{\rm pm2}$ turn ON and C_m and C_x are connected in parallel. During this stage, the voltage V_m is reduced as desired. Once sufficient charge has been removed from C_m, the series PMOS transistors are turned OFF and the fall in $V_{\rm inv}$ proceeds as before. When $V_{\rm inv}$ reaches near 0 V, the NMOS transistor M_n is turned ON. While M_n is ON, $V_{\rm inv}$ might be slightly negative or positive (not shown) due to the direction of the inductor current reversing and the ON-state resistance of the transistor. Afterward, a fast rising edge in $V_{\rm inv}$ is shown, as no ZVS turn-ON delay is employed for the PMOS transistor M_p in Fig. 6.

Signals $V_{\rm nmos}$ and $V_{\rm inv}$ are good candidates to drive $M_{\rm pm1}$ and $M_{\rm pm2}$ transistors, but preliminary simulation results show that a shifted $V_{\rm inv}$ with lower amplitude has a better timing. This leads to the use of $V_{\rm nmos}$ and $V_{\text{inv-shift}}$ as the gating signals. As shown in Fig. 8, $V_{\text{inv-shift}}$ is generated using a simple circuit that resembles a switched capacitor. When $V_{\rm inv} = V_{DD}$, capacitor $C_{\rm shift}$ is charged through diode $D_{\rm shift}$ to $V_{\rm shift} = V_{DD} - (V_m + V_{\rm diode})$. When $V_{\rm inv}$ is dropping, $D_{\rm shift}$ will become reverse-biased and $V_{\text{inv-shift}} = V_{\rm inv} - V_{\rm shift}$. With $V_{DD} = 2.2$ V, $V_m = 1.1$ V, and $V_{\rm diode} \cong 0.6$ V, then $V_{\rm shift} = 0.5$ V is achieved.

Also, the size of $M_{\rm pm2}$ is smaller than $M_{\rm pm1}$ to avoid loading a small chain (the lower chain) with a big PMOS gate. While the ratio of the transistor sizes is not optimal, as long as the sum

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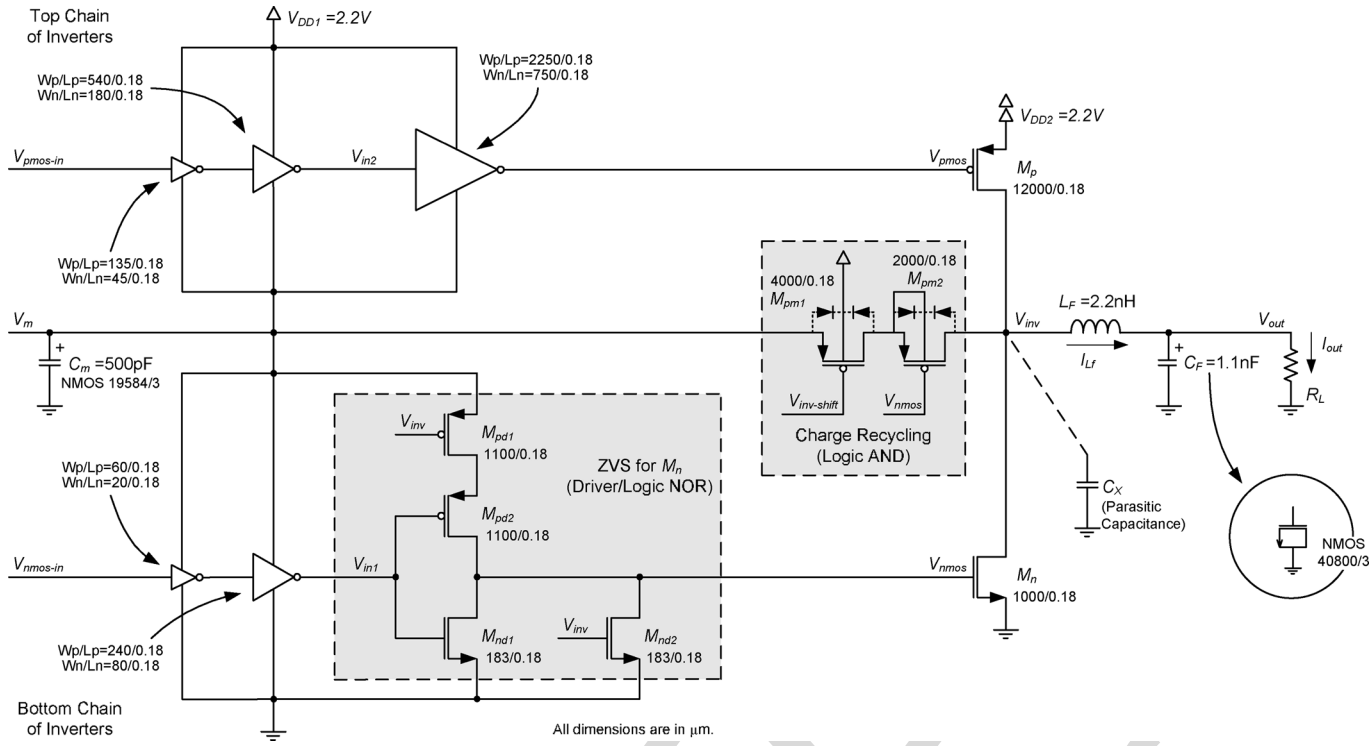

Fig. 6. Circuit diagram of the proposed ZVS and charge-recycling circuits for the dc–dc converter (coupling capacitors C_{c1} and C_{c2} are not shown for clarity).

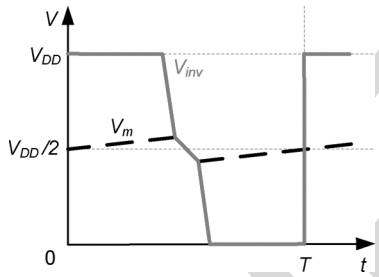

Fig. 7. Idealized timing diagram of the improved circuit diagram (ZVS on one edge only).

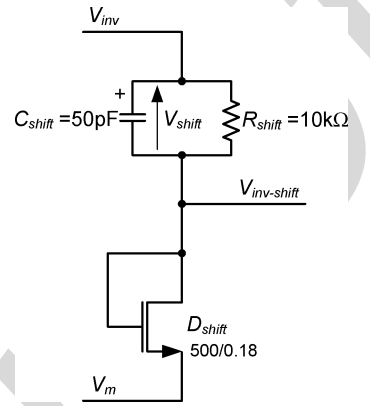

Fig. 8. Generating shifted voltage of $V_{\mathrm{inv\text{-}shift}}$.

of the series resistance is small, power loss in the recycling path will be low.

To disable the intrinsic body diodes, the body of M_{pm1} is connected to V_{DD}, which also increases its absolute threshold voltage value. This is another reason for using of $V_{\mathrm{inv\text{-}shift}}$ rather than V_{inv} as a gating signal. The body of M_{pm2} is connected to its source to keep the threshold voltage intact, but there are periods of time that its body diode is forward-biased. Since M_{pm1} is ON when V_{inv} is low, there would not be any current flowing from V_{inv} to V_m through the (forward biased) body diode of M_{pm2} and the (already turned on) transistor M_{pm1}.

2) Improved ZVS Operation: The effective duty cycle seen by the power circuit depends on various parameters, among which are the value of voltage V_m, the time delay needed to implement ZVS, and the existence of stray resistance, capacitance, and inductance in the actual circuit.

The NMOS ZVS implementation introduced in Fig. 6 is an improved version of the implementation presented by the authors in [4] and [6]. In that design, direct feedback from V_{inv} was used to drive the PMOS transistor that turns ON M_n. Because the gating signal to the NMOS transistor that turns OFF M_n was out of phase with the feedback signal, there could have been a period of time that both the driver PMOS and NMOS transistors are ON. To circumvent this problem, the supply to the lower driver inverter was taken from the V_{pmos} node, which was swinging between V_{DD} and zero.

In the circuit shown in Fig. 6, a complete logic NOR gate is implemented inside the driver inverter chain. This performs ZVS by gating M_{pd1} using V_{inv}. The two NMOS transistors in the logic can have the same size as the original inverter NMOS

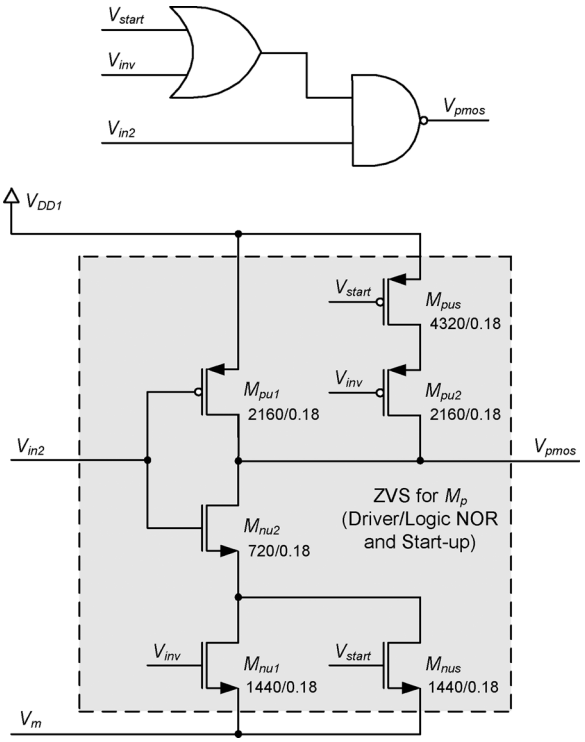

Fig. 9. ZVS logic and circuitry for M_p.

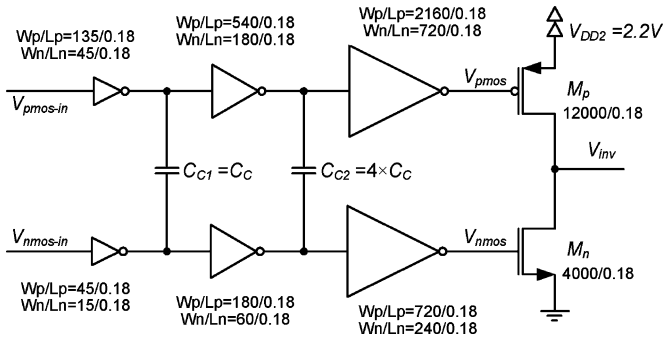

Fig. 10. Use of capacitive coupling to reduce skew.

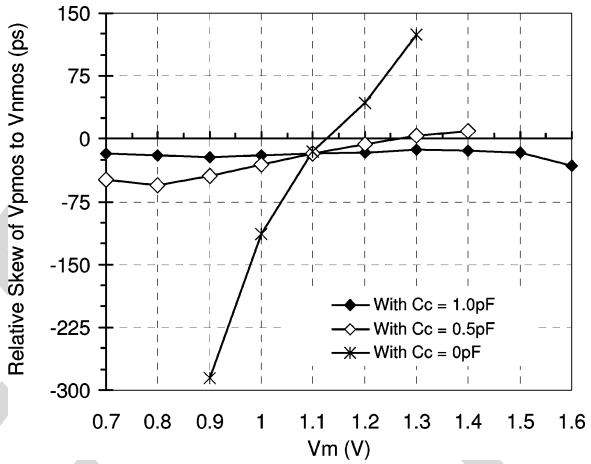

Fig. 11. Simulated effect of C_c on the relative skew of the gating signals.

transistor they replace, but the size of the PMOS transistors should be doubled to keep the drive effort as before.

In Fig. 6, size of the inductor L_F is reduced from 4.38 to 2.2 nH to increase the peak-to-peak value of the current in the inductor. This would increase the built-up current in L_F and facilitates the discharging/charging of C_x.

The ZVS circuit for the PMOS transistor M_p is the dual of the ZVS circuit for the NMOS transistor M_n and is shown in Fig. 9. To implement ZVS for M_p, a negative inductor current is needed. That means for a specific dc output current, a higher peak-to-peak inductor current will be observed; thus, the rms value of the current is increased, which will result in increased resistive losses in the system. On the other hand, ZVS for the PMOS transistor will reduce dynamic losses in the source–drain circuit of M_p and a smaller inductor is required. Thus, ZVS for PMOS may or may not provide a net reduction of power consumption depending on the operating conditions of the system.

It is necessary to disable the M_p ZVS circuitry and charge up C_x when no negative inductor current is present, such as at system start-up. At the start-up, the ZVS circuit must wait for the load voltage to rise so that a negative inductor current can occur to charge up C_x and bring up $V_{\rm inv}$. To detect start-up conditions, $V_{\rm out}$ can be sensed using a voltage comparator to produce the gating signal $V_{\rm start}$, which disables ZVS for M_p and charges C_x at the correct time.

3) Improved Half-Swing Gating Signal Propagation: In this improved design, the ZVS circuitry will automatically recycle charge and delay turning ON M_p or M_n according to conditions at $V_{\rm inv}$. This alleviates the need for external control signals to incorporate the required delays. Instead, control signals $V_{\rm pmos}$ and $V_{\rm nmos}$ should be as closely synchronized as possible. However, voltage supply mismatch caused by variation of V_m or noise in V_{DD} or ground can result in unequal propagation delays through the driver chains, causing $V_{\rm pmos}$ and $V_{\rm nmos}$ to arrive at different times than intended. In general, this condition is referred to as signal skew.

To circumvent skew, capacitive coupling is used to synchronize the signals [21] as shown in Fig. 10. The size of the coupling capacitors is determined such that when the signal in one side of the capacitor is changing, the other side will change as well.

The low-swing circuit of Fig. 10 is simulated with different values of C_c. As shown in Fig. 11, the use of coupling capacitors reduces the time difference between the rising edge of signals $V_{\rm pmos}$ and $V_{\rm nmos}$. Based on the curves in Fig. 11, a value of 1 pF is chosen for C_c, resulting in a short skew of about -20 ps between the two gating signals. However, in this short interval of time, both M_p and M_n are OFF, avoiding any possible short circuit from V_{DD} to the ground. Coupling capacitors $C_{c1} = 1$ pF and $C_{c2} = 4$ pF are also used in Fig. 6, but not shown here for clarity.

C. Simulation of the Improved Circuit

The fully featured circuit is simulated to provide voltage and current waveforms. The simulated circuit is shown in Fig. 6, except transistor sizes are slightly adjusted due to the use of

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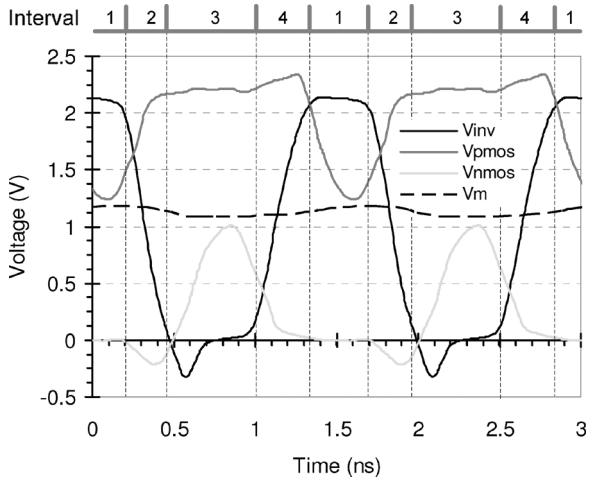

Fig. 12. Simulated voltage waveforms of Fig. 6 with M_p ZVS circuitry of Fig. 9 ($L_F = 1.1$ nH).

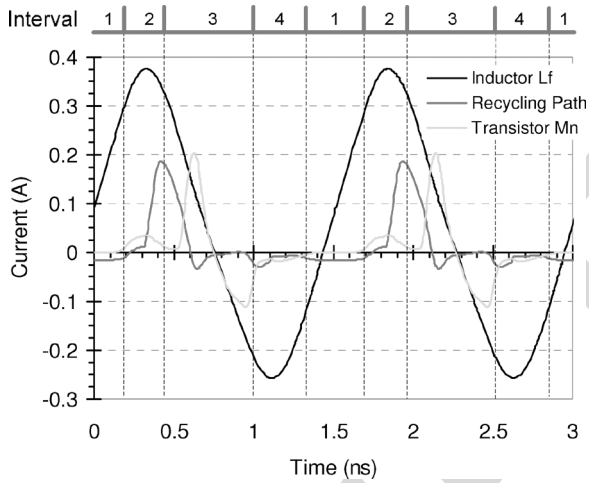

Fig. 13. Simulated current waveforms of Fig. 6 with M_p ZVS circuitry of Fig. 9 ($L_F = 1.1$ nH).

ZVS circuitry for M_p shown in Fig. 9. Simulated waveforms are provided in Figs. 12 and 13 running at $I_{\rm out} = 50$ mA, $D = 50\%$, and $L_F = 1.1$ nH with ZVS for M_p and M_n. In this simulation, the value of L_F is chosen so that a negative inductor current, which is needed for proper operation of ZVS for M_p, would be provided. At this operating point, $V_m = 1.13$ V, $V_{\rm out} = 0.95$ V, and $\eta = 38.3\%$. For proper operation of the circuit with ZVS for both M_p and M_n, the duty cycle range is limited between 50% and 60%. As can be observed in Fig. 12, the stacked low-swing driver design results in $V_{\rm pmos}$ swing between V_{DD} and $V_{DD}/2$, and $V_{\rm nmos}$ swing between $V_{DD}/2$ and zero. Also, note that these two gating signals are active at nonoverlapping times due to the ZVS circuitry. Comparing Fig. 12 to Fig. 13, the latter shows idealized voltage waveforms with $V_{\rm inv}$ at a higher than 50% duty cycle.

Fig. 13 shows the reversing inductor current. The current, which contains a net positive dc component, goes negative for the ZVS operation of M_p. Taken together with Fig. 12, which illustrates the delayed rise of $V_{\rm nmos}$ and the delayed fall of $V_{\rm pmos}$, this result indicates that ZVS operation for M_n and M_p is functioning correctly. In Fig. 13, the current through the recycling path and the current through M_n are out of phase, which indicates that recycled charge is not lost through M_n but it goes through the inductor to the load. In the graphs of Figs. 12 and 13, it should be noted that while the inductor current is smooth, transistor M_n current is not since the current is charging/discharging stray capacitances between the source and drain terminals of M_n.

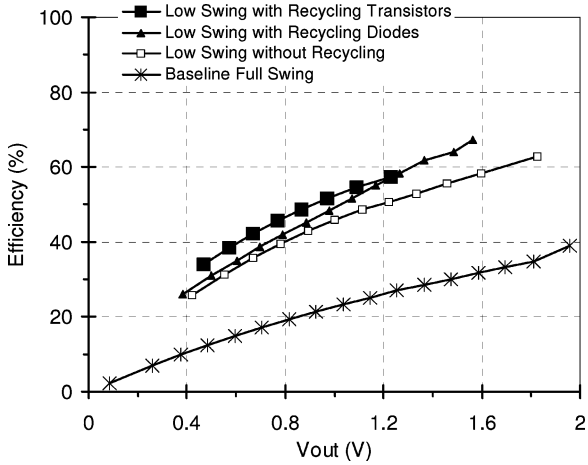

Fig. 14. Simulated efficiency versus output voltage for four variants of Fig. 6 ($L_F = 2.2$ nH).

To evaluate the benefits of driver charge recycling, four variants of the circuit were simulated: 1) baseline converter using two full-swing drivers; 2) low-swing/stacked drive chain is added and only ZVS for M_n is implemented; 3) recycling diode-connected NMOS transistors and C_m are added to 2) to recycle energy; and 4) recycling PMOS transistors and C_m are added to 2) to recycle energy. Only in 2), a supply voltage of $V_{DD}/2$ is connected to node V_m to keep it stable, otherwise V_m would rise. Simulations show that this voltage supply sinks (consumes) about 20 mA of current, which adds to the power consumption of the converter circuit itself.

Simulations of these four circuits are performed at a fixed load current of $I_{\rm out} = 100$ mA and $L_F = 2.2$ nH, and the results are shown in Figs. 14 and 15. In these simulations, the value of L_F is chosen so that the duty cycle range in which the converter circuit is operational with full swing $V_{\rm inv}$ is increased. As a result, ZVS for M_p is not employed since the inductor current does not reverse. The simulated waveforms were examined individually and data points corresponding to full swing $V_{\rm inv}$ are reported. ($V_{\rm inv}$ is considered to be full swing when its maximum value is above 2.0 V and its minimum value is below 0.2 V.) To make the task of comparing different variants of the circuit at each output voltage (and thus power) level easier, Fig. 14 shows efficiency as a function of output voltage while Fig. 15 shows the output voltage as a function of duty cycle.

As expected, the circuit with all the options 4) has the highest efficiency. Thus, using recycling transistors will improve the

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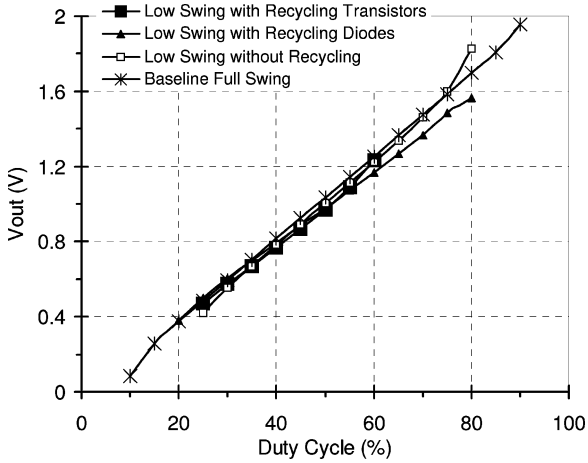

Fig. 15. Simulated output voltage versus duty cycle for four variants of Fig. 6 ($L_F = 2.2$ nH).

TABLE I
POWER CONSUMPTION BREAKDOWN OF FIG. 6 ($L_F = 2.2$ nH)

Component	Power (mW)
Total input power intake (taken from V_{DD1} and V_{DD2})	188
Power circuit intake (taken from V_{DD2})	137
Power circuit consumption (adding up the losses in power circuit components and the output power)	145
Driver circuit power intake (taken from V_{DD1}) (includes top and bottom chains, M_n ZVS circuitry and recycling path transistors M_{pm1} and M_{pm2})	50
Top chain power intake (taken from V_{DD1} with respect to V_m)	21
Bottom chain power intake (taken from V_m) (includes M_n ZVS circuitry)	13
Recycling path PMOS transistors M_{pm1} and M_{pm2} losses	16
Transistor M_p losses	38
Transistor M_n losses (under ZVS operation)	2.5
Capacitor C_F losses	Negligible
Inductor L_F losses	7.5
Output power delivered (to load R_L)	97

efficiency compared to the other variants of the circuit. Also, using low-swing drivers with ZVS for M_n will improve the efficiency compared to the full-swing circuit. The baseline full swing has the worst performance. For example, at an output voltage of 1 V, the efficiency of the circuits are: 1) baseline: 22%; 2) low-swing drivers with ZVS: 46%; 3) low-swing drivers with ZVS and energy recycling diode-connected NMOS transistors: 49%; and 4) low-swing drivers with ZVS and energy recycling PMOS transistors: 52%. Thus, the efficiency improves from 22% to 52% with the energy-saving design methodology of using low-swing drivers with ZVS and energy recycling PMOS transistors. While the ZVS circuitry improves the efficiency of the circuit, the added components to implement ZVS still contribute to the driver losses. Thus, it is important to keep the ZVS timing circuitry neat and simple.

Simulated power consumption of various components of the circuit in Fig. 6, at nominal output current of 100 mA and 50% duty cycle, with $L_F = 2.2$ nH and ZVS for M_p disabled, is shown in Table I. Power circuit components are M_p, M_n, L_F, C_F, and the load. As in other simulations in this paper, an ASITIC [15] extracted model and an NMOS transistor model are used for the inductor L_F and for the capacitor C_F, respectively, which ensures that the parasitic losses of these components are accounted for. For the power circuit, power taken from V_{DD2} is less than power calculated by adding up the output power and losses in the power circuit components, because there is a second path for energy to get into the power circuit and that is through the recycling transistors, confirming the functioning energy recycling. The driver circuit consists of the top and bottom chain of inverters, including M_n ZVS circuitry and recycling path transistors $M_{\rm pm1}$ and $M_{\rm pm2}$. The driver circuit is the biggest single consumer of power with 50 mW, justifying our close attention to this part of the circuit. Power transistor M_p is the second highest with 38 mW and the recycling transistors path is third with 16 mW power consumption. Because of the ZVS operation, the transistor M_n is ON for a shorter period of time, and when ON, it has a lower current level; thus, it consumes only 2.3 mW. In this simulation, the power consumption of the top chain is less than twice the bottom chain. The reasons are that although the size of the top chain is about twice the bottom chain, V_m is higher than $V_{DD}/2$ and the ZVS circuitry consumes some power itself.

The circuit of Fig. 6 is basically a buck converter, with a reversing but effectively continuous current in the inductor. In (4), f_c denotes the corner frequency of the output *LC* filter [14]. Simulation results confirm that the output ripple is around 5% for all variants of the circuit

$$\frac{\Delta V_{\rm out,pp}}{V_{\rm out}} = \frac{\pi^2}{2}(1-D)\left(\frac{f_c}{f_{\rm sw}}\right)^2. \tag{4}$$

V. CONCLUSION

The low-swing buck converter design presented here demonstrates the operation of a 660 MHz converter implemented in a 0.18 μm process, including ON-chip passives. The measured efficiency obtained is promising for such a prototype and for such a high switching frequency. However, the most important result is that energy recycling has been shown to be an essential and practical way to reduce energy loss in the front-end drive chain and boost overall conversion efficiency. An improved recycling circuitry was also proposed that further improves the efficiency of the implemented circuit. The lack of low-V_t transistors in the prototype reduced the effectiveness of the energy saving, although some saving is evident. Low-V_t transistors are expected to be increasingly available in standard design kits as the methods employed here become commonplace.

The chip area consumed by the converter is dominated by the inductance even at 660 MHz. The ON-chip inductor in the fabricated circuit was designed for an rms current of 50 mA. This represents a power to area ratio of 50 mW/2.5 mm^2.

Ultimately, the switching frequency has to be increased to reduce the size of the passive components, making ON-chip filter components practical. While this implies more switching losses, the steps presented here to reduce the driver power losses mitigate the adverse effects of a high switching frequency. Consequently, it is expected that such high-frequency designs will become of interest in a wide range of integrated circuit applications. The principles developed here are part of a range of low-energy methods, which will in time allow chips to be powered in an efficient way.

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